DS2401
Silicon Serial Number

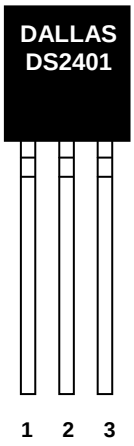
www.maxim-ic.com

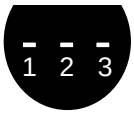
FEATURES

- Upgrade and drop-in replacement for DS2400
  - — Extended 2.8 to 6.0 voltage range
  - — Multiple DS2401s can reside on a common 1-Wire® Net
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester); guaranteed no two parts alike
- Built-in multidrop controller ensures compatibility with other 1-Wire Net products
- 8-bit family code specifies DS2401 communications requirements to reader
- Presence Pulse acknowledges when the reader first applies voltage
- Low-cost TO-92, SOT-223, and TSOC surface mount packages
- Reduces control, address, data, and power to a single pin
- Zero standby power required
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
- TO-92 Tape & Reel version with leads bent to 100mil spacing (default) or with straight leads (DS2401T-SL)
- Applications
  - — PCB Identification
  - — Network Node ID
  - — Equipment Registration
- Operates over industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT

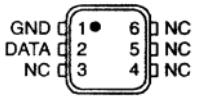
TO-92





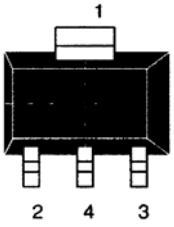
BOTTOM VIEW

TSOC PACKAGE

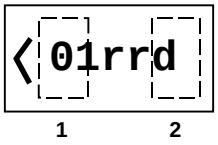


TOP VIEW
3.7mm x 4.0mm x 1.5mm

SOT–223



TOP VIEW
See Mech. Drawings Section



Flip Chip, Top View
with Laser Mark,
Contacts Not Visible.
"rrd" = Revision/Date

See 56-G7009-001 for package outline.

PIN DESCRIPTION

	TO-92, SOT-223	TSOC	Flip Chip
Pin 1	Ground	Ground	Data (DQ)
Pin 2	Data (DQ)	Data (DQ)	Ground
Pin 3	No Connect	No Connect	—
Pin 4	Ground	No Connect	—
Pin 5-6	—	No Connect	—

1-Wire is a registered trademark of Dallas Semiconductor.

ORDERING INFORMATION

Standard	Lead-Free	Description
DS2401	DS2401+	TO-92 Package
DS2401/T&R	DS2401+T&R	TO-92 Package, Tape-and-Reel
DS2401/T&R/SL	DS2401-SL+T&R	TO-92 Package with Straight Leads, Tape-and-Reel
DS2401Z	DS2401Z+	SOT-223 Surface-Mount Package
DS2401Z/T&R	DS2401Z+T&R	SOT-223 Surface-Mount Package, Tape-and-Reel
DS2401P	DS2401P+	TSOC Surface-Mount Package
DS2401P/T&R	DS2401P+T&R	TSOC Surface-Mount Package, Tape-and-Reel
DS2401X1	—	Flip-Chip Package, Tape & Reel

DESCRIPTION

The DS2401 enhanced Silicon Serial Number is a low-cost, electronic registration number that provides an absolutely unique identity which can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The DS2401 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol that requires only a single data lead and a ground return. Power for reading and writing the device is derived from the data line itself with no need for an external power source. The DS2401 is an upgrade to the DS2400. The DS2401 is fully reverse-compatible with the DS2400 but provides the additional multi-drop capability that enables many devices to reside on a single data line. The familiar TO-92, SOT-223 or TSOC package provides a compact enclosure that allows standard assembly equipment to handle the device easily.

OPERATION

The DS2401's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS2401 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing).

Hardware Configuration

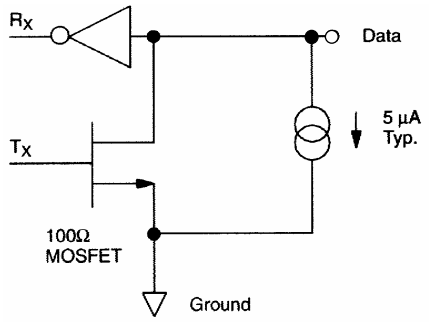
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open-drain connection or 3-state outputs. The DS2401 is an open-drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pullup resistor should be approximately 5kΩ for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbits per second.

The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus may be reset.

DS2401 MEMORY MAP Figure 1

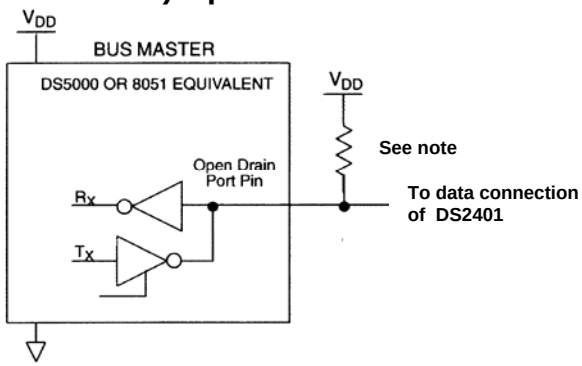
8-Bit CRC Code	48-Bit Serial Number	8-Bit Family Code (01h)
MSB LSB	MSB LSB	MSB LSB

DS2401 EQUIVALENT CIRCUIT Figure 2

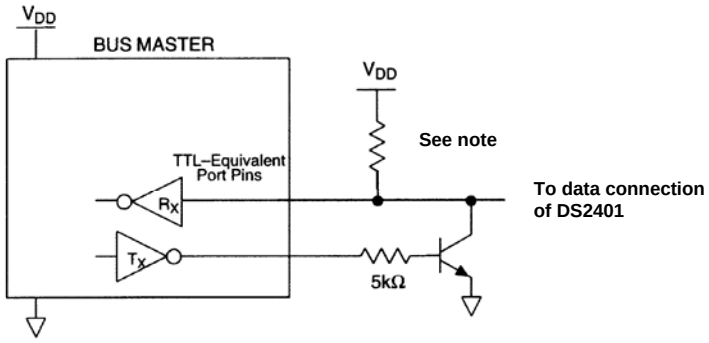


BUS MASTER CIRCUIT Figure 3

A) Open Drain



B) Standard TTL



Note:
Depending on the 1-Wire communication speed and the bus load characteristics, the optimal pullup resistor (R_{PU}) value will be in the 1.5kΩ to 5kΩ range.

TRANSACTION SEQUENCE

The sequence for accessing the DS2401 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that the DS2401 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 4).

Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS2401's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2401 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The DS2401 Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS2400, which will only respond to a 0Fh command word with its 64-bit ROM data.

Match ROM [55h] / Skip ROM [CCh]

The complete 1-Wire protocol for all Dallas Semiconductor iButtons contains a Match ROM and a Skip ROM command. Since the DS2401 contains only the 64-bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1-Wire bus if executed. The DS2401 does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (for example, a DS2401 and DS1994 on the same bus).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See *Application Note 187: 1-Wire Search Algorithm* for a comprehensive discussion of a ROM search, including an actual example.

1-WIRE SIGNALING

The DS2401 requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All these signals except Presence Pulse are initiated by the bus master.

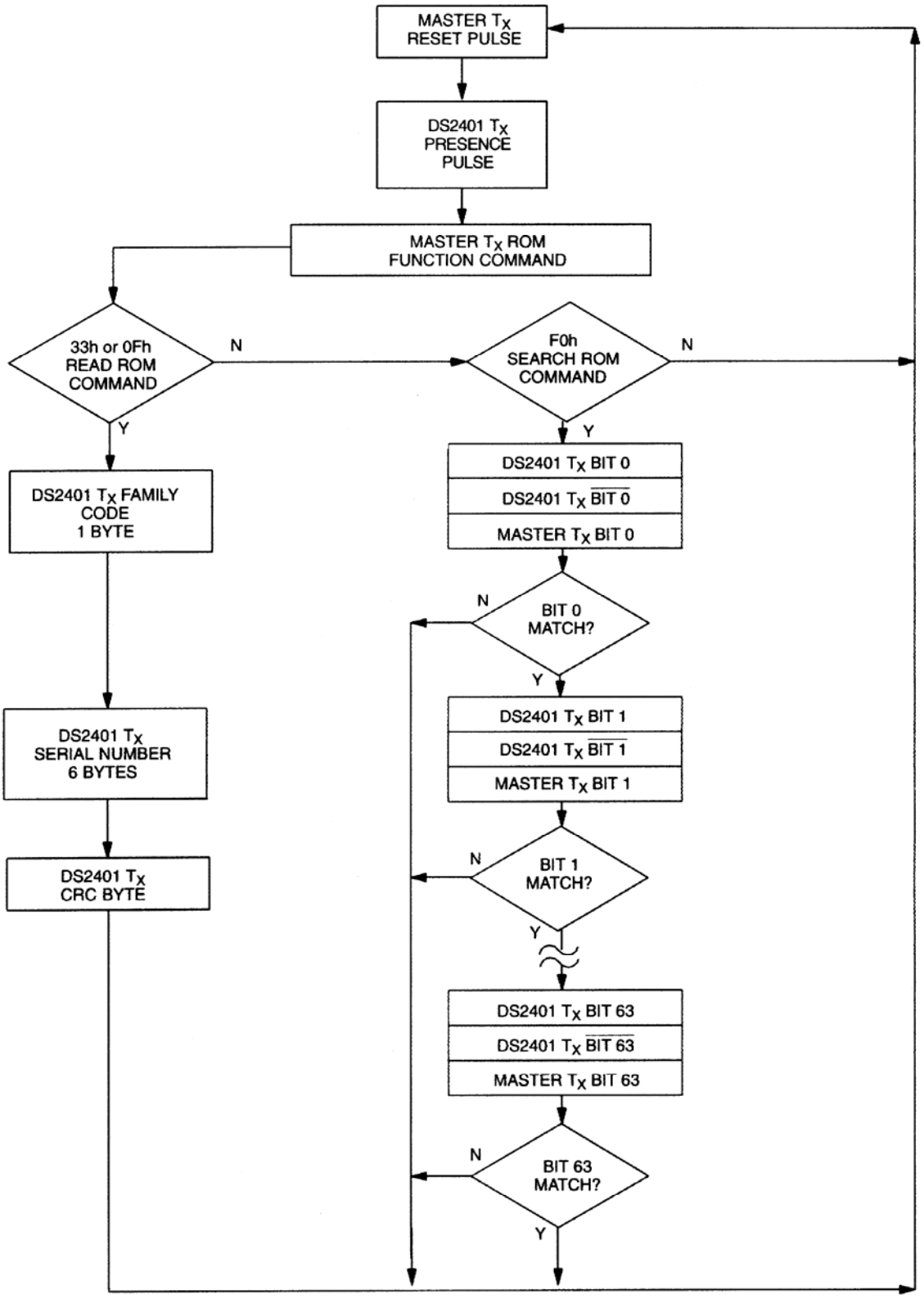
The initialization sequence required to begin any communication with the DS2401 is shown in Figure 5. A reset pulse followed by a Presence Pulse indicates the DS2401 is ready to send or receive data given the correct ROM command.

The bus master transmits (T_X) a reset pulse (t_{RSTL}, minimum 480µs). The bus master then releases the line and goes into receive mode (R_X). The 1-Wire bus is pulled to a high state via the 5kΩ pullup resistor. After detecting the rising edge on the data pin, the DS2401 waits (t_{PDH}, 15-60µs) and then transmits the Presence Pulse (t_{PDL}, 60-240µs). The 1-Wire bus requires a pullup resistor range of 1.5kΩ to 5kΩ, depending on bus load characteristics.

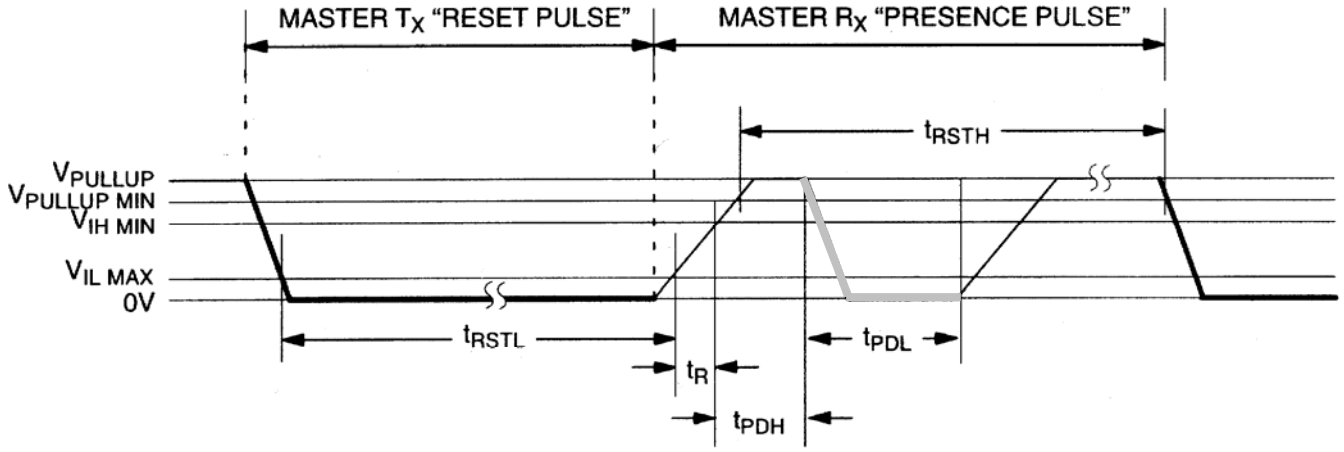
READ/WRITE TIME SLOTS

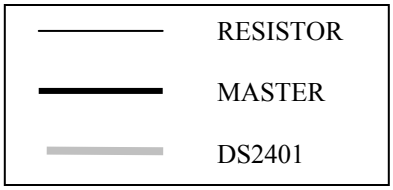
The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2401 to the master by triggering a delay circuit in the DS2401. During write time slots, the delay circuit determines when the DS2401 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2401 will hold the data line low overriding the "1" generated by the master. If the data bit is a 1, the DS2401 will leave the read data time slot unchanged.

ROM FUNCTIONS FLOW CHART Figure 4



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



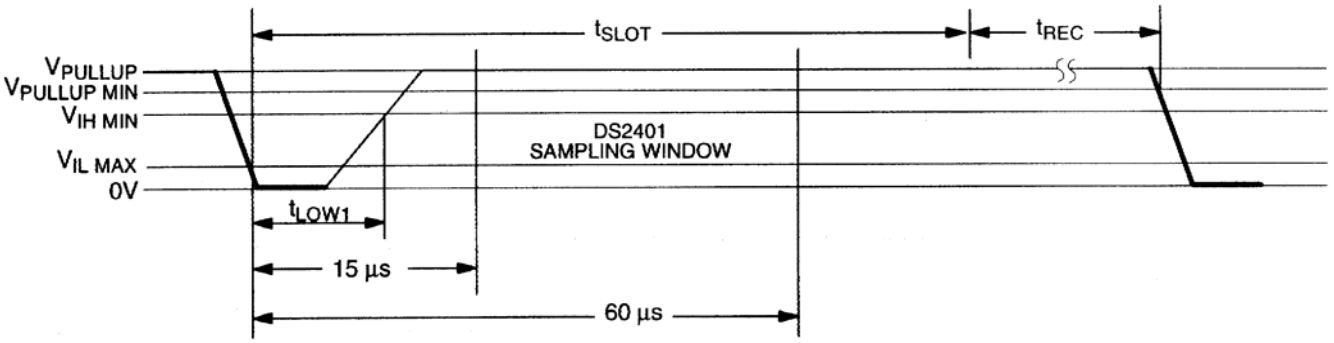


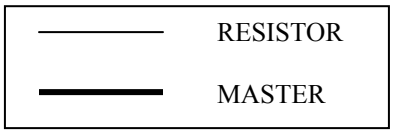
$480\mu s \le t_{RSTL} < \infty$ *
$480\mu s \le t_{RSTH} < \infty$ (includes recovery time)
$15\mu s \le t_{PDH} < 60\mu s$
$60\mu s \le t_{PDL} < 240\mu s$

* In order not to mask interrupt signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960µs.

READ/WRITE TIMING DIAGRAM Figure 6

Write-One Time Slot

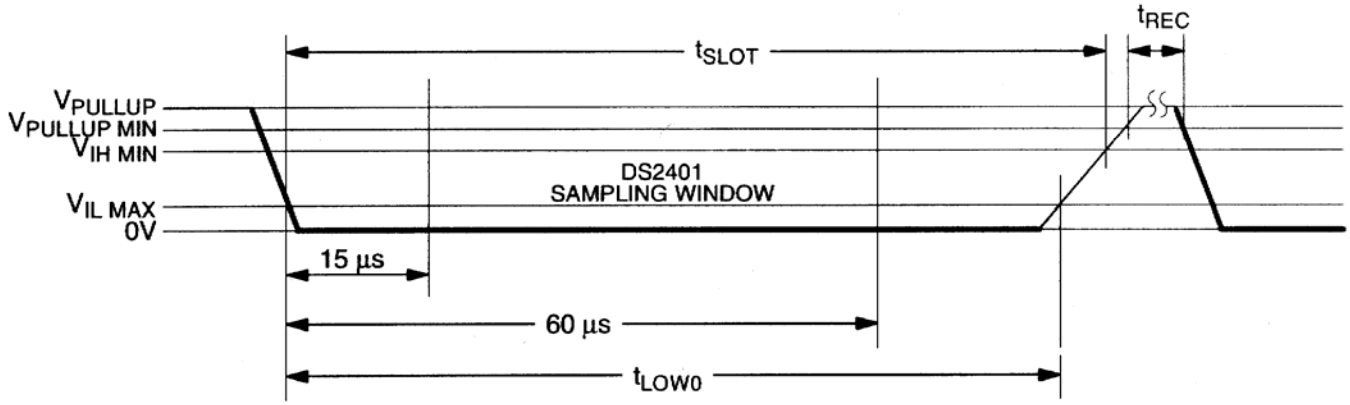




$60\mu s \le t_{SLOT} < 120\mu s$
$1\mu s \le t_{LOW1} < 15\mu s$
$1\mu s \le t_{REC} < \infty$

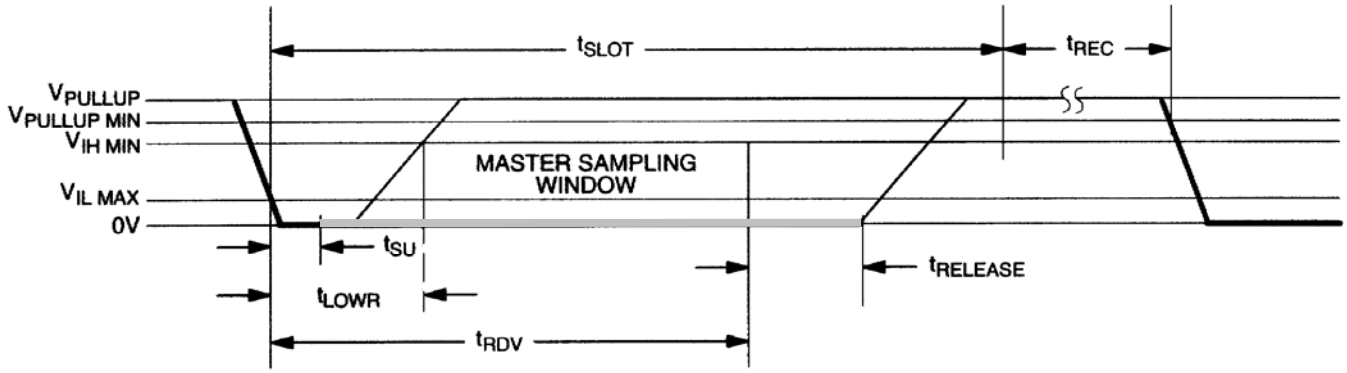
READ/WRITE TIMING DIAGRAM (cont'd) Figure 6

Write-zero Time Slot



$60\mu s \le t_{LOW0} < t_{SLOT} < 120\mu s$
$1\mu s \le t_{REC} < \infty$

Read-data Time Slot



$60\mu s \le t_{SLOT} < 120\mu s$
$1\mu s \le t_{LOWR} < 15\mu s$
$0 \le t_{RELEASE} < 45\mu s$
$1\mu s \le t_{REC} < \infty$
$t_{RDV} = 15\mu s$
$t_{SU} < 1\mu s$

CRC GENERATION

To validate the data transmitted from the DS2401, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the DS2401. If the two CRC values match, the transmission is error-free.

The equivalent polynomial function of this CRC is: $CRC = x^8 + x^5 + x^4 + 1$. Additional information about the Dallas 1-Wire CRC is available in *Application Note 27*.

CUSTOM DS2401

Customization of a portion of the unique 48-bit serial number by the customer is available. Dallas Semiconductor will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your Dallas Semiconductor sales representative for more information.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} = 2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1,6
Logic 0	V_{IL}	-0.3		+0.3	V	1
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1,2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7,8

CAPACITANCE (t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} = 2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	12
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		15		µs	11
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	10
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1) All voltages are referenced to ground.

2) V_{PUP} = external pullup voltage.

3) Input load is to ground.

4) An additional reset or communication sequence cannot begin until the reset high time has expired.

5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge and will remain valid for 14µs minimum (15µs total from falling edge on 1-Wire bus).

6) V_{IH} is a function of the external pullup resistor and the V_{CC} supply.

7) 30 nanocoulombs per 72 time slots @ 5.0V.

8) At V_{CC} = 5.0V with a 5kΩ pullup to V_{CC} and a maximum time slot of 120µs.

9) Capacitance on the I/O pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pullup the I/O line to V_{CC}, 5µs after power has been applied the parasite capacitance will not affect normal communications.

10) The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise it could mask or conceal interrupt pulses if this device is used in parallel with a DS2404 or DS1994.

11) The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.

12) The duration of the low pulse sent by the master should be a minimum of 1µs with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.