XAPP854 (v1.0) October 10, 2006

Digital Phase-Locked Loop (DPLL) Reference Design

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Summary

Many applications require a clock signal to be synchronous, phase-locked, or derived from another signal, such as a data signal or another clock. This type of clock circuit is important in many communications or audio video applications to keep data synchronized. In a digital FPGA-based system, this function often uses external mixed-signal ICs, which add additional cost, power, and complexity to the system. This application note and reference design provide a digital phase-locked loop (DPLL) solution that utilizes spare resources in a Virtex™-4 FPGA and requires minimal external components. The performance of the DPLL is superior to most integrated mixed-signal solutions. The DPLL design can be used in many different applications, including jitter reduction PLLs, clock multiplier PLLs, clock recovery PLLs, and clock generators.

Introduction

Figure 1 is a block diagram of the DPLL reference design. In addition to the Virtex-4 FPGA, the design requires two external components: a low-cost digital-to-analog converter (DAC) and a voltage-controlled oscillator (VCO). Many trade-offs can be made when choosing the DAC and the VCO.

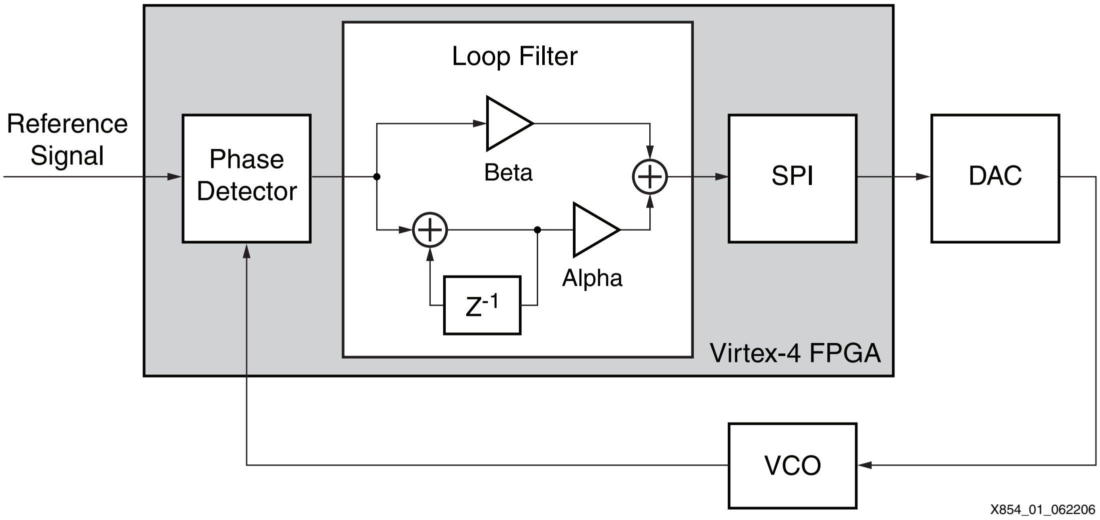

Figure 1: **DPLL Block Diagram**

Resolution and DAC speed are key attributes to consider for performance. The higher the resolution, the lower the quantization noise and jitter contribution due to the DAC. However, a 12-bit DAC such as the Analog Devices AD5320 is sufficient in most applications. Speed is the limiting factor in how fast the loop can update. The speed of the DAC is limited by the speed of the interface and the slew rate of the output voltage. The interface speed is most important because, during a lock condition, the output voltage does not deviate significantly. The slew rate affects the loop's ability to lock to a signal and stay locked to a signal in the presence of noise.

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The VCO performance dictates the performance of the PLL. Because the loop bandwidth of the DPLL is very low, the output noise of the PLL is approximately the same as the intrinsic noise of the VCO output. Another factor to consider is the VCO gain. The lowest gain possible should be selected to meet the design requirements. Reducing the gain of the VCO reduces the effect of DAC resolution and update rate.

The data and testing results in this application note were gathered with an Analog Devices AD5320 12-bit DAC and a Crystek CVPD-024 156.25 MHz Voltage Controlled Crystal Oscillator. In quantities greater than 1000, the DAC cost is $2.50 per device and the VCXO cost is $28. Lower cost oscillators are available from vendors such as Pletronics, Vectron, and Silicon Labs.

Design

The DPLL FPGA design consists of a phase detector, a loop filter, a serial peripheral interface, and a VCO. The phase detector (`pd.v`) tells the PLL which direction to operate and at what speed. The reference design contains two phase detector variants. The first is the accumulating bang-bang phase detector. All data in this application note is based on this phase detector unless otherwise stated. The other variants is a frequency detector (`fd.v`).

The gain associated with the loop filter (`lp.v`) keeps the loop locked and affects many of the PLL attributes. The loop filter consists of two separate gain paths. The first-order path controls the response to small changes in phase, and the second-order path maintains the DC bias and tracks the slower, larger changes in frequency. The first-order gain is controlled by the 8-bit digital control beta. The second-order gain is controlled by the 8-bit digital control alpha.

The serial peripheral interface (`spi.v`) communicates the digital control voltage from the FPGA into the DAC. The designer must modify this block to support the DAC selected for the user application. The DPLL reference design supports only the AD5320. The VCO provides the clocking circuitry for the blocks in the design.

The reference design also provides a ChipScope™ Pro VIO core to monitor and control the DPLL circuit. This core enables the monitoring of the digital control voltage and other key signals as well as control of key parameters, such as alpha, beta, and clock dividers.

Figure 2 shows the DPLL FPGA design.

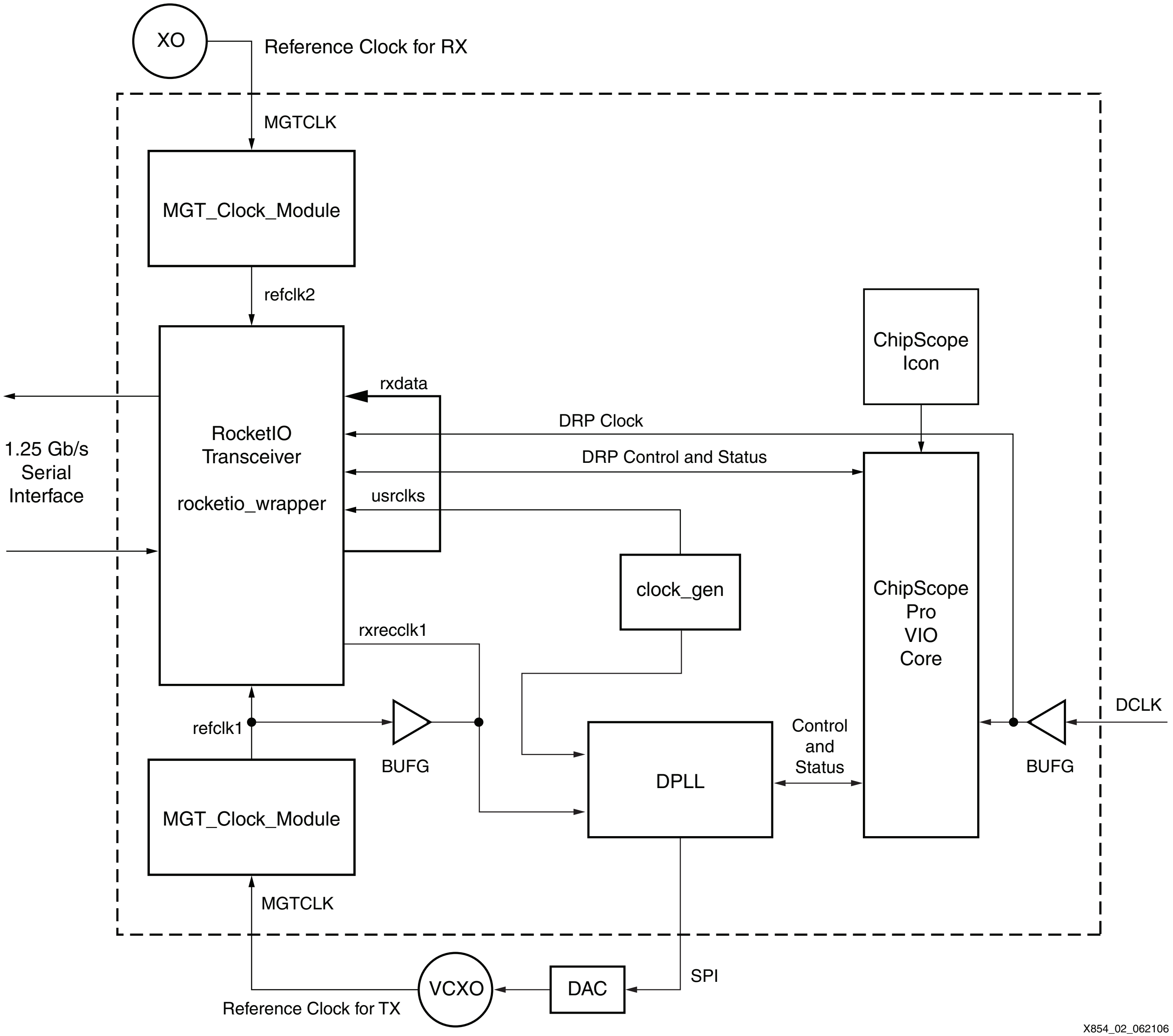
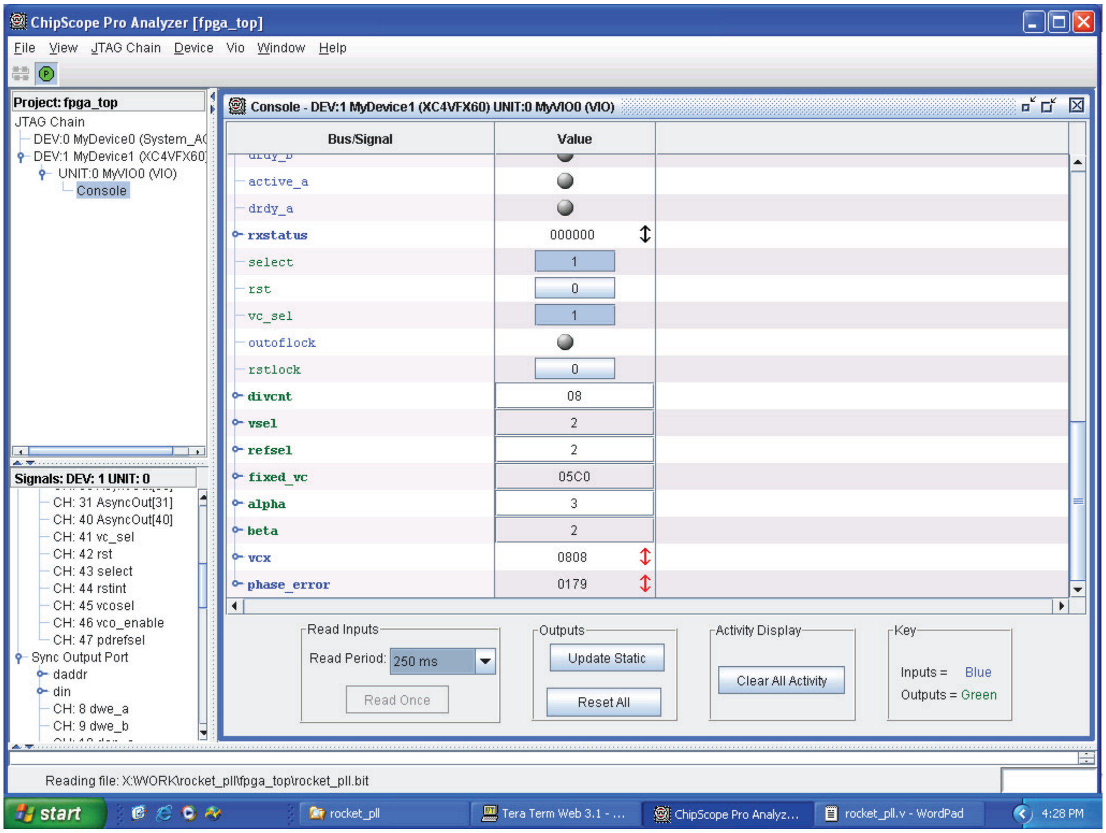


Figure 2: **DPLL FPGA Block Diagram**

ChipScope Control and Status

Figure 3 is a screen capture from the ChipScope tool.



Bus/Signal	Value
drdy_b	●
active_a	●
drdy_a	●
rxstatus	000000 ↕
select	1
rst	0
vc_sel	1
outoflock	●
rstlock	0
divcnt	08
vsel	2
refsel	2
fixed_vc	05C0
alpha	3
beta	2
vcx	0808 ↕
phase_error	0179 ↕

Read Period: 250 ms

Reading file: X:\WORK\rocket_pll\fpga_top\rocket_pll.bit

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Figure 3: **ChipScope Screen Capture**

Table 1 summarizes the accessible control and status signals on the ChipScope core in alphabetical order.

Table 1: **ChipScope Core Control and Status Signals**

Name	Control/Status	Description
Active_a	Status	Indicates that the calibration block is active for MGT A
Active_b	Status	Indicates that the calibration block is active for MGT B
Alpha	Control	Controls the second-order gain control
Beta	Control	Controls the first-order gain control
Daddr	Control	Connects to the address port of the DRP interface for MGT A and MGT B
Dcm_locked	Status	Status indicating that the DCM in the clock_gen block is locked
Dcmreset	Control	Resets the DCM in the clock_gen block, which is used to generate MGT USRCLKs
Den_a	Control	Connects to the den port of DRP interface of MGT A
Den_b	Control	Connects to the den port of DRP interface of MGT B
Din	Control	Connects to the data input port of the DRP interface of MGT A and MGT B
Disable_a	Control	Disables the MGT A calibration block

Table 1: **ChipScope Core Control and Status Signals *(Continued)***

Name	Control/Status	Description
Disable_b	Control	Disables the MGT B calibration block
Divcnt	Control	Controls the divider for the DAC serial interface
Do_a	Status	Connects to the data output port of the DRP interface for MGT A
Do_b	Status	Connects to the data output port of the DRP interface for MGT B
Drdy_a	Status	Indicates that the DRP data output is available for MGT A
Drdy_b	Status	Indicates that the DRP data output is available for MGT B
Dwe_a	Control	Connects to the dwe port of DRP interface of MGT A
Dwe_b	Control	Connects to the dwe port of DRP interface of MGT B
Fixed_vc	Control	Fixed DAC value used when vc_sel = 0
Outoflock	Status	Latched out of lock indicator 1 = Out of lock 0 = Locked
Phase_error	Status	Indicates the value from either the phase detector or the frequency detector
Refsel	Control	Selects a bit of the frequency detector's reference counter
Rst	Control	Resets the DPLL logic
Rstlock	Control	Clears the latch for the out of lock indicator
Rx_reset	Control	Resets the MGT TX digital logic
Rxbufferr	Status	Indicates a buffer error occurred inside the RX of MGT A
Rxclkstable	Control	Connects to rxclkstable of the MGT
Rxlock	Status	Indicates that the RX PLL of MGT A is locked
Rxpmareset	Control	Resets the MGT RX PMA block
Rxsig_detect	Control	Connects to the RX signal detect pin of the MGT
Rxstatus	Status	Connects to the rxstatus bus of MGT A
Select	Control	1 = Selects the frequency detector 0 = Selects the phase detector
tx_reset	Control	Resets the MGT TX digital logic
Txbufferr	Status	Indicates a buffer error occurred inside the TX of MGT A
Txclkstable	Control	Connects to the txclkstable input of the MGT
Txlock	Status	Indicates that the TX PLL of MGT A is locked
Txpmareset	Control	Resets the MGT TX PMA block
Txsig_detect	Control	Connects to the TX signal detect pin of the MGT
Vc_sel	Control	1 = Normal closed loop 0 = Fixed control voltage
Vcx	Status	Indicates the control voltage value
Vsel	Control	Selects a bit of the frequency detector's VCO counter

Implementation

This section describes the two basic implementations of the DPLL and presents their testing results.

Accumulating Bang-Bang Phase Detector

The accumulating bang-bang phase detector (ACBBPD) is a mainstream implementation. It works well in most applications, including clock and data recovery, jitter reduction, and clock multiplication. It does not, however, work with the clock from the digital CDR of the RocketIO™ transceiver or the fabric-based digital oversampling CDRs, whose clock transitions are derived from an asynchronous reference clock.

Figure 4 shows the complete ABBPD implementation.

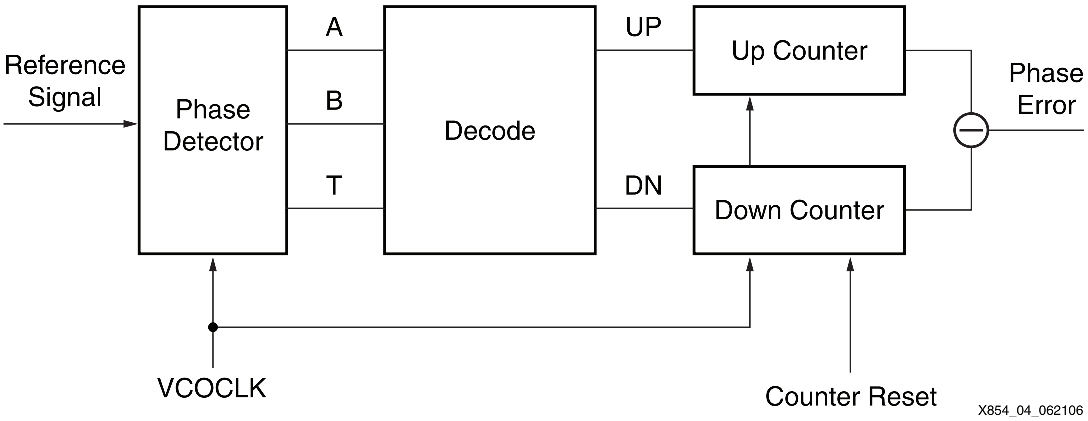

Figure 4: **Accumulating Bang-Bang Phase Detector**

Figure 5 provides more details of the ABBPD phase detector block.

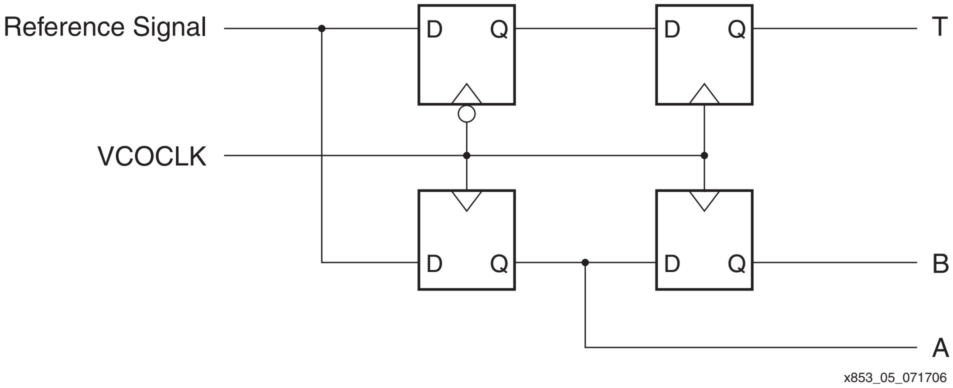

Figure 5: **Bang-Bang Phase Detector**

The reference signal can be a data signal or a clock signal. If it is a clock signal, it must be at least half the rate of the VCOCLK rate. Connecting this phase detector with the loop filter and other components implements a robust DPLL. The loop filter controls the loop bandwidth and stability. The basic operating parameters must follow these rules:

1. Beta must be less than alpha – 3.
2. The larger the alpha and beta, the lower the bandwidth and the longer the lock time.
3. Beta must be less than 8.
4. VCOCLK/divcnt must be less than the maximum SCLK frequency.

The plots in Figure 6 through Figure 9 show the performance of the DPLL using the ABBPD. It was tested standalone without a RocketIO transceiver, using a signal generator as a reference signal.

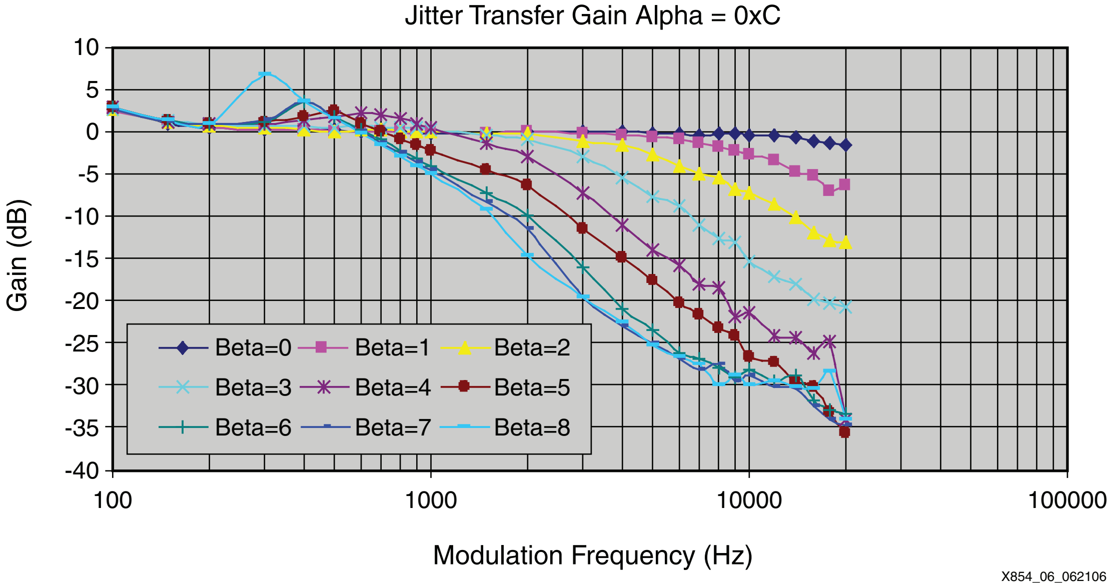

Figure 6: **Jitter Transfer with Fixed Alpha**

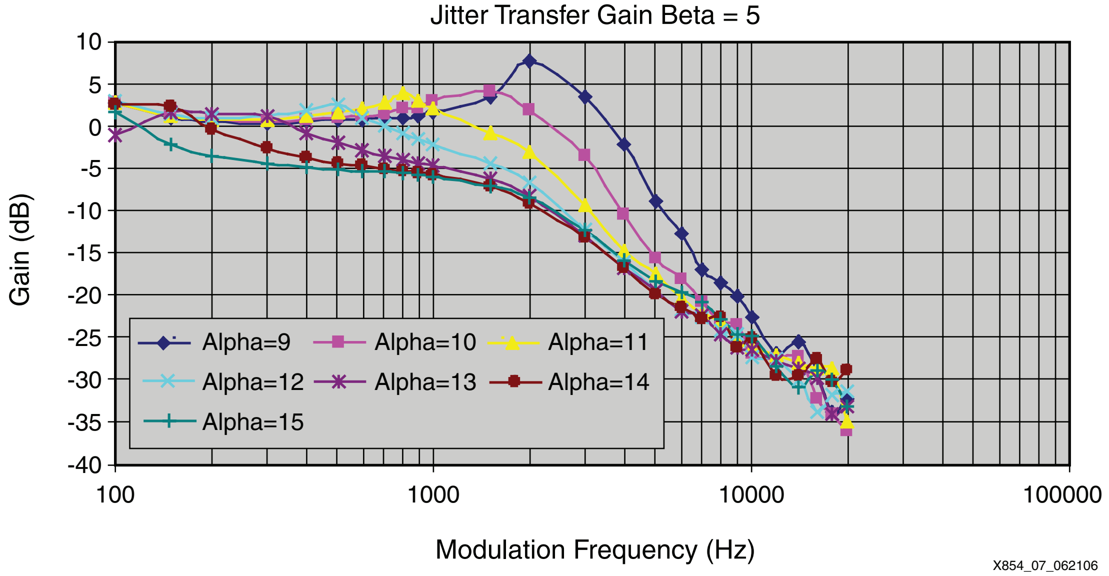

Figure 7: **Jitter Transfer Fixed Beta**

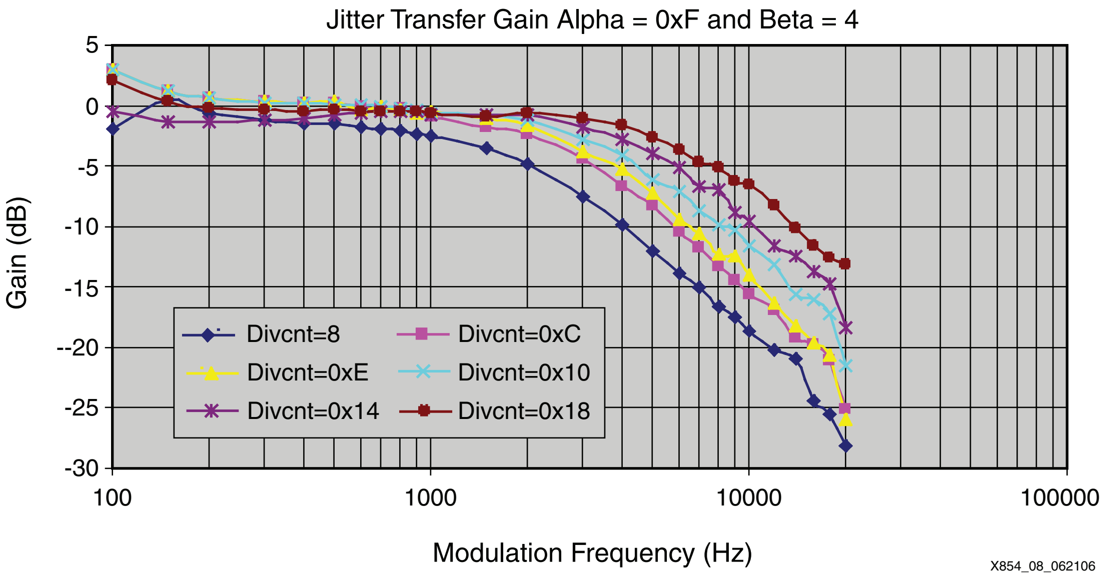

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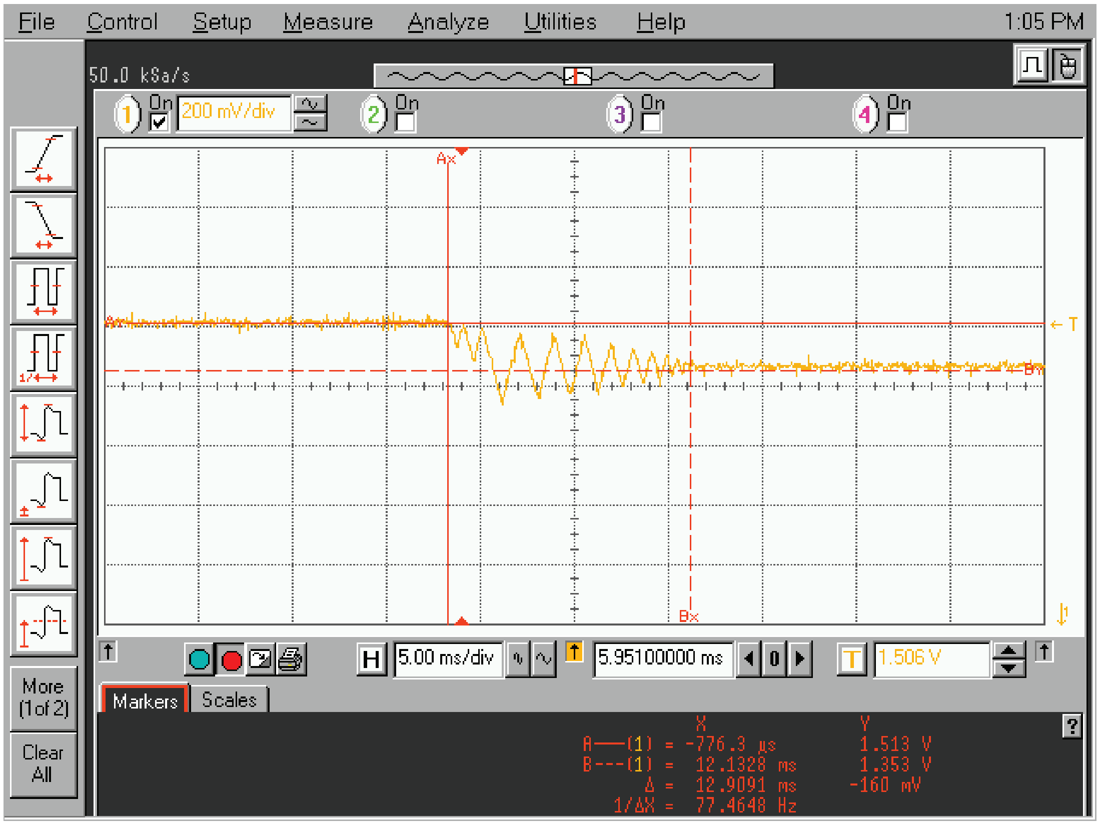
Figure 8: **Jitter Transfer Fixed Alpha and Beta**



```
                  X                    Y
A——(1) = -776.3 µs              1.513 V
B---(1) =  12.1328 ms           1.353 V
      Δ =  12.9091 ms          -160 mV
   1/ΔX =  77.4648 Hz
```

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Figure 9: **Negative 1000 Hz Frequency Step Response (Alpha = 9 and Beta = 5)**

Frequency Detector

The frequency detector implementation is used in cases that the ABBPD cannot handle, such as with a clock that is digitally derived via a digital oversampling CDR.

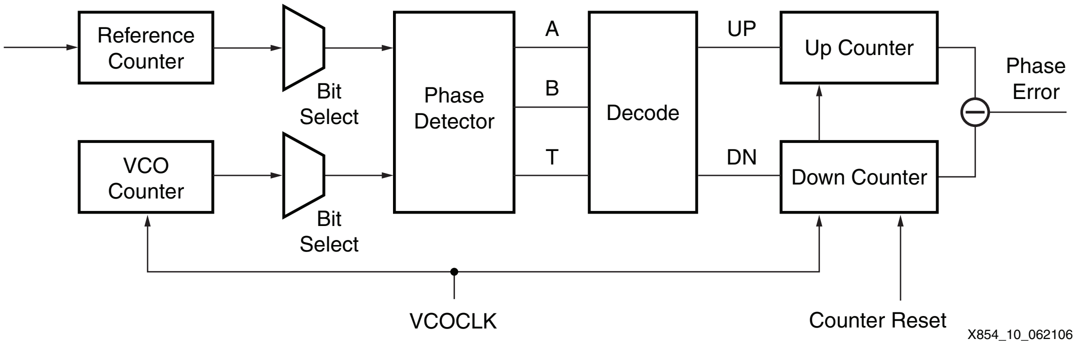
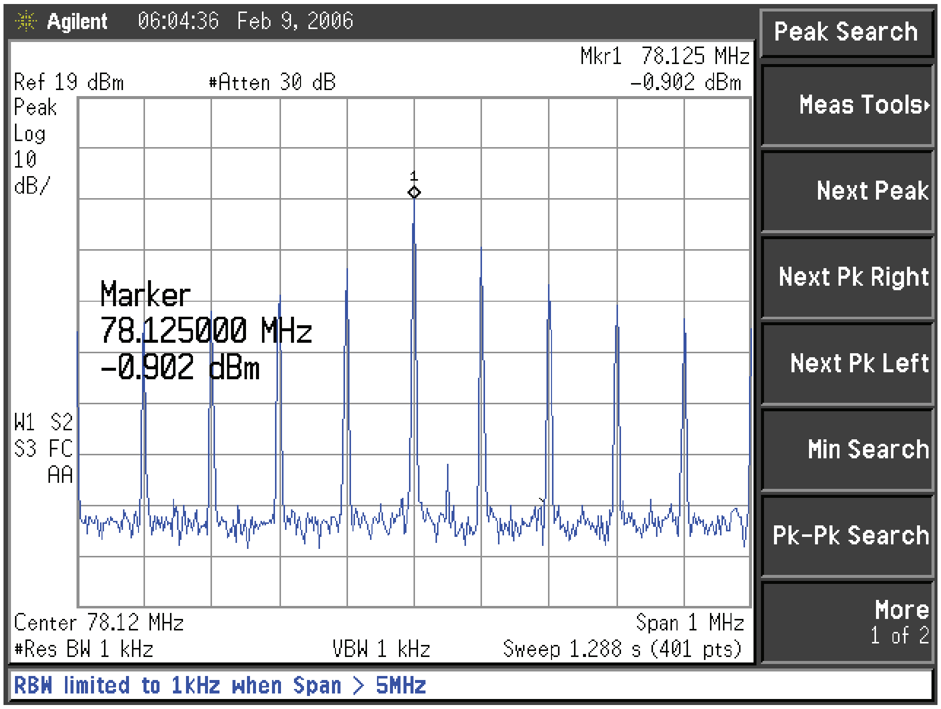


Figure 10: **Frequency Detector**

With the addition of a reference counter and a VCO counter, the phase detector can determine which counter is accumulating clock pulses faster than the other. The counters are relatively small; however, because they are not reset and effectively rollover, they behave like infinitely large counters. The bit select provides one of the counter bits to the phase detector. Selecting a high-order bit in a traditional system results in a dramatic reduction in phase detector gain. However, the accumulators in the phase detector, which are clocked from the VCOCLK, compensate for this gain, resulting in a more uniform gain for the phase detector regardless of which counter bit is selected. Bit selection is programmable or selectable during loop operation, and changes do not result in loss of lock. Selection of lower counter bits provides fast acquisition, while selection of higher bits results in more immunity from instantaneous phase jumps of the reference signal due to the nature of digital oversampled CDR operation.

Figure 11 shows the spectral content of the RXRECCLK from the digital oversampled CDR with large sideband spurs.


Agilent 06:04:36 Feb 9, 2006

Mkr1 78.125 MHz
-0.902 dBm

Ref 19 dBm #Atten 30 dB

Peak
Log
10
dB/

Marker
78.125000 MHz
-0.902 dBm

W1 S2
S3 FC
AA

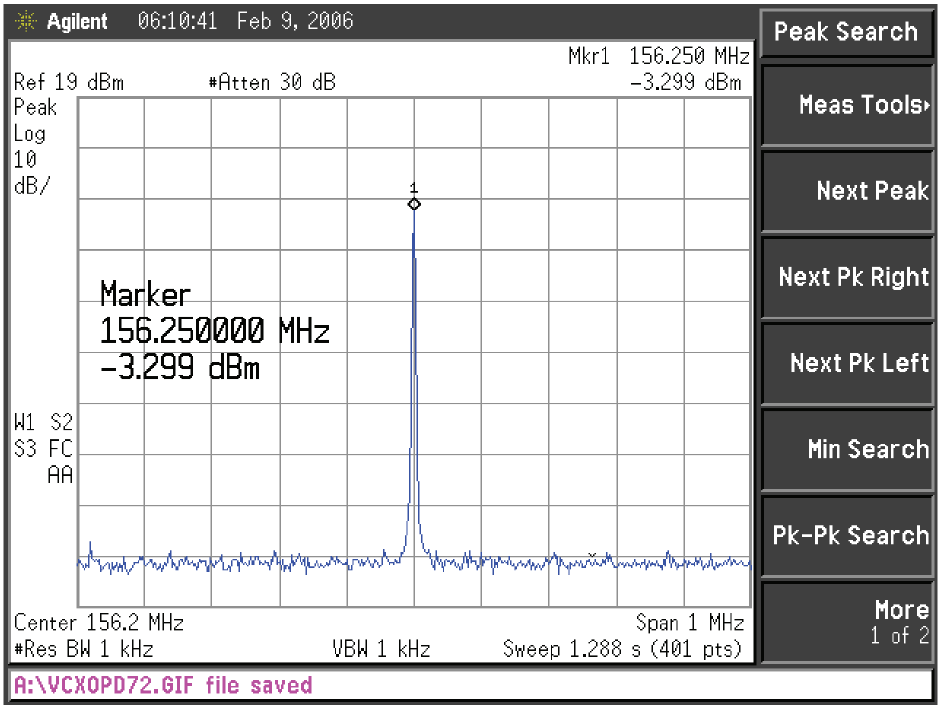
Center 78.12 MHz Span 1 MHz
#Res BW 1 kHz VBW 1 kHz Sweep 1.288 s (401 pts)

RBW limited to 1kHz when Span > 5MHz

X854_11_062106

Figure 11: **Spectral Plot of Digital CDR RXRECCLK**

Figure 12 shows the VCXO clock of the DPLL when using the frequency detector.



Agilent 06:10:41 Feb 9, 2006

Mkr1 156.250 MHz
-3.299 dBm

Ref 19 dBm #Atten 30 dB
Peak
Log
10
dB/

Marker
156.250000 MHz
-3.299 dBm

W1 S2
S3 FC
AA

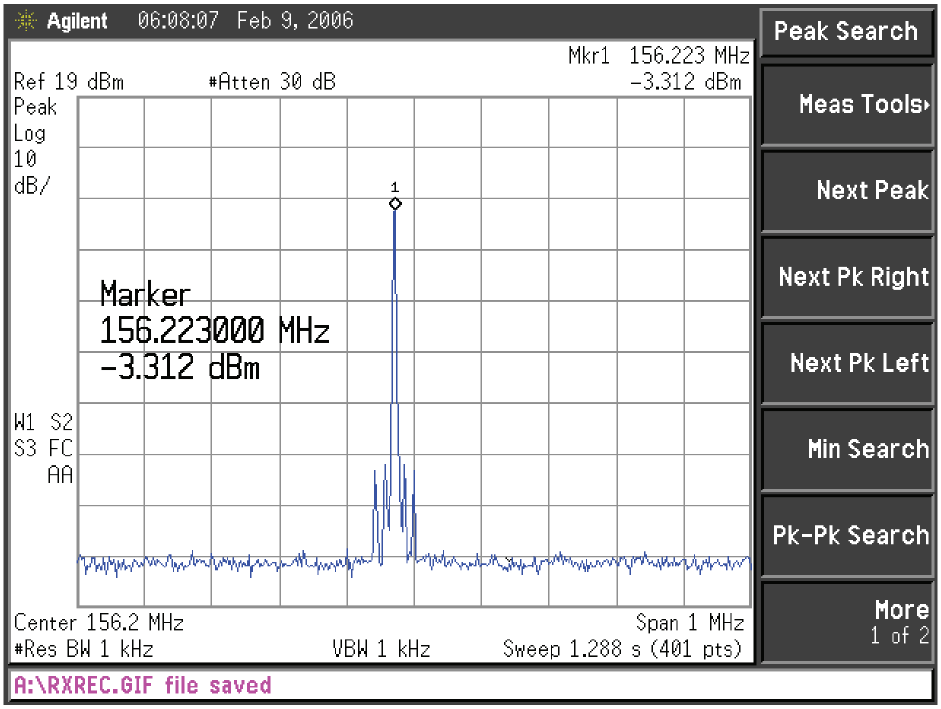
Center 156.2 MHz Span 1 MHz
#Res BW 1 kHz VBW 1 kHz Sweep 1.288 s (401 pts)

A:\VCXOPD72.GIF file saved

X854_12_062106

Figure 12: **Spectral Plot of VCXO of DPLL Using Frequency Detector**

Figure 13 shows the same VCXO clock when using the phase detector. The DPLL is not properly locked to the correct frequency when using the phase detector circuit alone.



Agilent 06:08:07 Feb 9, 2006

Mkr1 156.223 MHz
-3.312 dBm

Ref 19 dBm #Atten 30 dB
Peak
Log
10
dB/

Marker
156.223000 MHz
-3.312 dBm

W1 S2
S3 FC
AA

Center 156.2 MHz Span 1 MHz
#Res BW 1 kHz VBW 1 kHz Sweep 1.288 s (401 pts)

A:\RXREC.GIF file saved

X854_13_062106

Figure 13: **Spectral Plot of VCXO of DPLL Using the Phase Detector**

Reference Design

The reference design contains all the Verilog source and Xilinx project files needed to build the test system and migrate into a customer-specific design. The directory structure is listed below:

`xapp854`

- `coregen`: Directory containing coregen generated IP
  - `rocketio_wrapper`: RocketIO Wizard generated core
  - `clock_gen`: DCM Wizard generated core
- `chipscope`: ChipScope components
  - `fpga_top.cpj`
- `fpga_top`: Project navigator directory
  - `fpga_top.ucf`: UCF
  - `fpga_top.ise`: Project navigator project file
- `src`: Verilog source files
  - `rocket_pll.v`: Top-level design with RocketIO transceiver and ChipScope tool
  - `dpll.v`: DPLL design
  - `lp.v`: Loop filter design
  - `spi.v`: Interface logic to DAC
  - `vcodiv.v`: Dividers etc. for DAC and other counters
  - `pd.v`: Accumulating bang-bang phase detector
  - `fd.v`: Frequency detector

The DPLL reference design can be downloaded from the Xilinx website at http://www.xilinx.com/bvdocs/appnotes/xapp854.zip.

Conclusion

The DPLL reference design enables a user to implement two PLL types using Virtex-4 FPGAs. The design test results show very low noise and the ability to lock to and filter noise associated with the digital oversampled CDR of the RocketIO transceiver. Some experimentation is required to derive the most effective first-order and second-order gain constants for each user's application; however, with the flexibility of the reference design, most applications can be supported. This design has been implemented effectively in video and communications applications.

Additional References

The following references provide additional information useful to this application note:

- UG024, *RocketIO Transceiver User Guide*
- UG029, *ChipScope Pro Software and Cores User Guide*
- XAPP514, *Audio/Video Connectivity Solutions for the Broadcast Industry*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/10/06	1.0	Initial Xilinx release.