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Digilent XC95 Reference Manual

Overview

The Digilent XC95 development board featuring the Xilinx 95108 CPLD provides an inexpensive and expandable platform on which to design and implement basic digital circuits. The board can also be used to program other Digilent peripheral boards (such as the DIO2 board) that contain CPLD devices. DXC95 board features include:

- A Xilinx 95108 CPLD with 108 macrocells;
- An on-board 1.5A, 5VDC power regulator;
- A socketed 1.842MHz oscillator;
- A JTAG-based programming port using a standard parallel cable;
- A status LED and pushbutton for basic I/O;
- Two 100-mil spaced, right-angle DIP socket 40-pin expansion connectors.

The DXC95 board has been designed specifically to work with the Xilinx ISE CAD tools, including the free WebPack tools available from the Xilinx website. Like other in the Digilab family, the DXC95 board has been partitioned so that only the hardware required by a particular project need be purchased. Several peripheral boards that mate with the expansion connectors are available, such as the DIO1 board that provides several basic I/O devices (see www.digilentinc.com for more information). The low-cost, standard expansion connectors allow new peripheral boards, including wire-wrap or manually soldered boards, to be quickly designed and used. The DXC95 board ships with a power supply and programming cable, so designs can be implemented immediately without the need for any additional hardware.

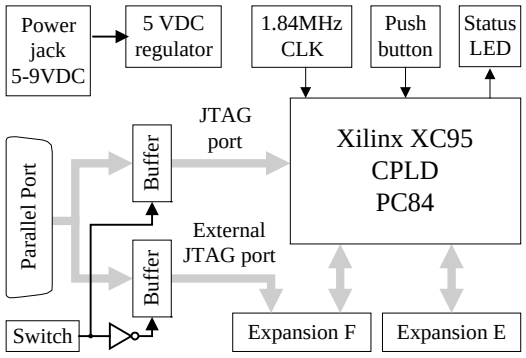


Figure 1. DXC95 board schematic

Functional description

The Digilab DXC95 board has been designed to offer a low-cost and minimal system for designers who need a flexible platform to gain exposure to Xilinx CPLDs, or for those who need to prototype CPLD-based designs rapidly. The DXC95 board also has an external JTAG port – in a lower-cost configuration, the board can be used to program Digilab peripheral boards (such as the DIO2 or AIO1 boards). The DXC95 board provides only the essential supporting devices for the 95108 CPLD, and routes all available CPLD signals to standard expansion connectors. Included on the board are a 5VDC regulator, a JTAG configuration circuit that uses a standard parallel cable, a 1.8MHz oscillator, and a pushbutton and LED for rudimentary I/O.

The DXC95 board has been designed to serve as a host for various peripheral boards. The expansion connectors on the board mate with standard 40-pin, 100 mil spaced DIP headers available from any catalog distributor. Each of the expansion connectors provides the unregulated supply voltage (VU), 5V, GND, and 37 CPLD signals to peripheral boards, so system designers can quickly develop application- specific peripheral boards. Digilent also produces a collection of expansion boards with commonly used devices. See the Digilent website (www.digilentinc.com) for a listing of currently available boards.

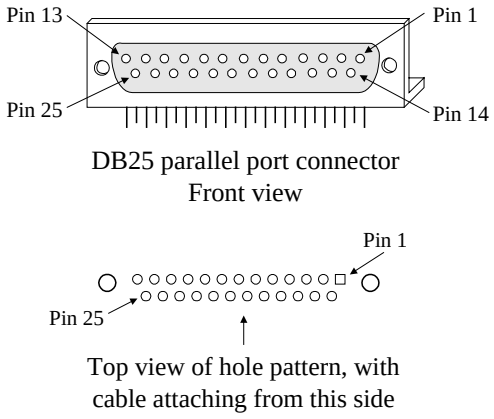
Power Supplies	
VU	Unregulated power supply voltage – depends on power supply used. Must be between 5VDC and 10VDC. Routed to regulators and expansion connectors only.
VCC	VCC for all devices, routed on inner PCB plane. 1.5A can be drawn with less than 20mV ripple (typical)
GND	System ground routed to all devices on PCB ground plane
Programming and parallel port	
PWT	Feedback of TDO signal
PPO	Cable detect signals used by Xilinx programmer
TMS-L	Local TMS signal (used for JTAG programming)
TCK-L	Local TCK signal (used for JTAG programming)
TDI-L	Local TDI signal (used for JTAG programming)
TMS-F	External TMS signal (used for JTAG programming)
TCK-F	External TCK signal (used for JTAG programming)
TDI-F	External TDI signal (used for JTAG programming)
On board devices	
BTN1	Pushbutton input
LED1	User-controllable status LED
MCLK	CMOS oscillator connected to global clock input
Expansion Connectors	
E4-E40	E bus signals connecting the E connector to the FPGA
F4-F40	F bus signals connecting the F connectors to the FPGA

Table 1. DXC95 board signal definitions

Table 1 shows all signals routed on the DXC95 board. These signals and their circuits are described in the following sections.

Parallel port and FPGA configuration circuit

The DXC95 board uses a DB-25 parallel port connector to route JTAG programming signals from a host computer to the CPLD and to the F expansion connector. Three-state buffers, controlled by an user-settable switch, determine whether the JTAG port is mapped to the on-board device or to the expansion connector. With this circuit, the on-board CPLD or a peripheral board CPLD can be configured using the JTAG protocol over the parallel cable. The JTAG programming circuit follows the schematic available from Xilinx, so the DXC95 board is fully compatible with all Xilinx programming tools. The JTAG circuit is shown in the diagram below.



Pin	EPP signal	EPP Function
1	Write Enable (O)	Low for read, High for write
2-9	Data bus (B)	Bidirectional data lines
10	Interrupt (I)	Interrupt/acknowledge input
11	Wait (I)	Bus handshake; low to ack
12	Spare	NOT CONNECTED
13	Spare	NOT CONNECTED
14	Data Strobe (O)	Low when data valid
15	Spare	NOT CONNECTED
16	Reset (O)	Low to reset
17	Address strobe (O)	Low when address valid
18-25	GND	System ground

Figure 1. Parallel port connectors and signals

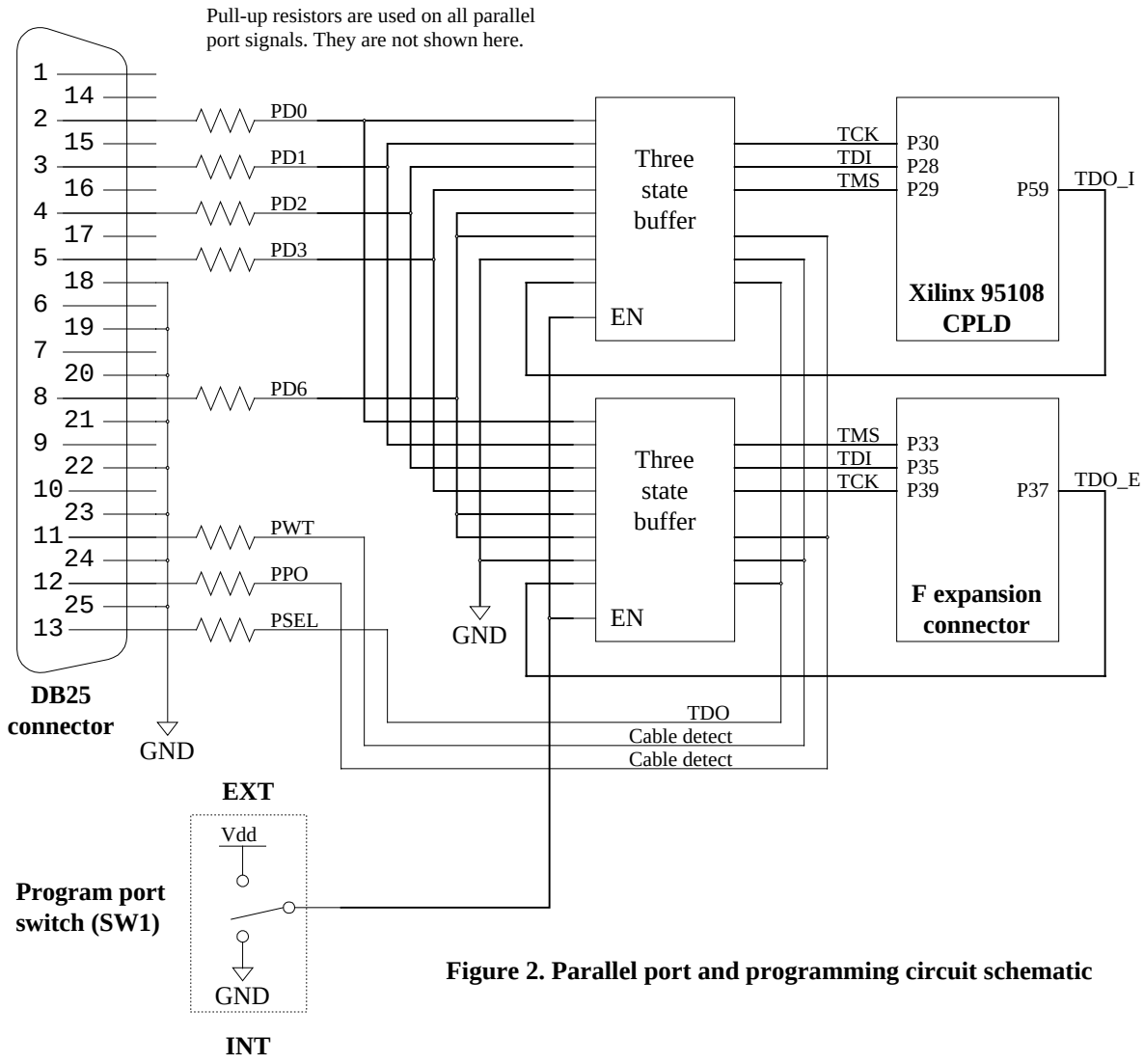


Figure 2. Parallel port and programming circuit schematic

Oscillator

The DXC95 board provides a socketed half-size 8-pin DIP oscillator. The board ships with a 1.8MHz oscillator, but oscillators from 32KHz to 50MHz can easily be substituted, allowing for a wide range of clock frequencies. The oscillator is connected to the CPLD GCK1 input (P9), it is bypassed with a 0.1uF capacitor, and it located as physically close to the CPLD as possible.

Power Supplies

The DCX95 board uses a 1.5A LM317 LDO voltage regulator to produce the 5VDC supply. The regulator input is driven from an external DC power supply connected to the on-board 2.1mm center-positive power jack. The regulator has 10uF of input capacitance, 20uF of local output capacitance, and 10uF of regulation bypass capacitance. The regulator produces a stable, low noise supply using inexpensive wall-wart power supplies, regardless of load (up to 1.5A). The regulator body is soldered to the board for improved thermal dissipation. DC supplies in the range of 5VDC to 10VDC may be used. Ample bypass capacitors are used around the board to decrease power supply noise. The DXC95 board uses a four layer PCB, with the inner layers dedicated to VCC and GND planes

Total board current is dependant on CPLD configuration, clock frequency, and external connections. In test circuits with approximately half the CPLD resources routed, a 1.8MHz clock source, and a single expansion board attached (the DIO1 board), approximately 300mA of supply current is drawn from the supply. Current is strongly dependent on CPLD and peripheral board configurations.

Pushbutton and LED

A single pushbutton and LED are provided on the board allowing basic status and control functions to be implemented without a peripheral board. As examples, the LED can be illuminated from a signal in the CPLD to verify that configuration has been successful, and the pushbutton can be used to provide a basic reset function independent of other inputs. The circuit is shown below.

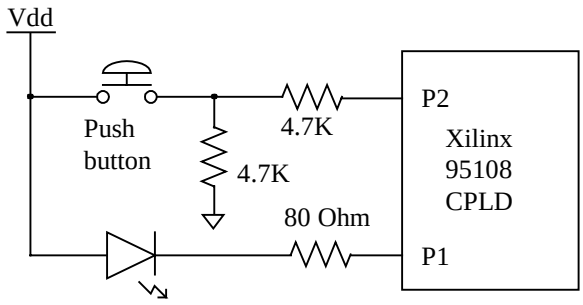
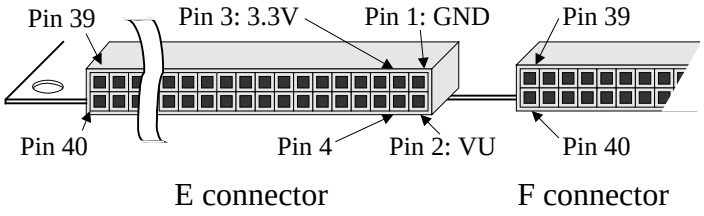


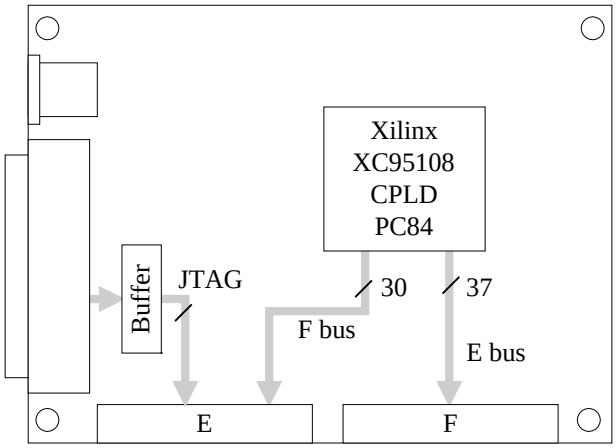
Figure 5. Pushbutton and LED detail

Expansion connectors



The two expansion connectors labeled E and F on the DXC95 board use 100 mil spaced DIP headers. Both connectors have GND routed to pin 1, VU routed to pin 2, and 5V routed to pin 3. Pins 4-40 for both connectors route directly to individual CPLD pins. The connectors are separated by 400 mils, so any Digilent peripheral board can be used with the DCX95 board.

The PC84 package used on the DXC95 board has 69 signal pins available to the user (the remaining pins are used for VCC, GND, and JTAG). Of these, 69, 3 are used for the button, led, and clock, and the rest are routed to the E and F peripheral connectors. Data rates of up to the full clock frequency are attainable across the E and F connectors.



DXC95 expansion connector signals

DXC95 Expansion Connector Pinouts					
E connector			F connector		
Pin	Signal	XC95 pin	Pin	Signal	XC95 pin
1	GND	-	1	GND	-
2	VU	-	2	VU	-
3	VDD33	-	3	VDD33	-
4	E4	84	4	F4	36
5	E5	83	5	F5	35
6	E6	82	6	F6	34
7	E7	81	7	F7	33
8	E8	80	8	F8	32
9	E9	79	9	F9	31
10	E10	75	10	F10	26
11	E11	72	11	F11	25
12	E12	71	12	F12	24
13	E13	70	13	F13	23
14	E14	69	14	F14	21
15	E15	68	15	F15	20
16	E16	67	16	F16	19
17	E17	66	17	F17	18
18	E18	65	18	F18	17
19	E19	63	19	F19	15
20	E20	62	20	F20	14
21	E21	61	21	F21	13
22	E22	58	22	GCLK3	12
23	E23	57	23	F23	11
24	E24	56	24	GCLK2	10
25	E25	55	25	F25	7
26	E26	54	26	F26	6
27	E27	53	27	F27	5
28	E28	52	28	F28	4
29	E29	51	29	F29	3
30	E30	50	30	BTN1	2
31	E31	48	31	MCLK	9
32	E32	47	32	LED1	1
33	E33	46	33	TMS_F	29
34	E34	45	34	GTS1	76
35	E35	44	35	TDI_F	28
36	E36	43	36	GSR	74
37	E37	41	37	TDO_F	59
38	E38	40	38	GTS2	77
39	E39	39	39	TCK_F	30
40	E40	37	40	F40	-

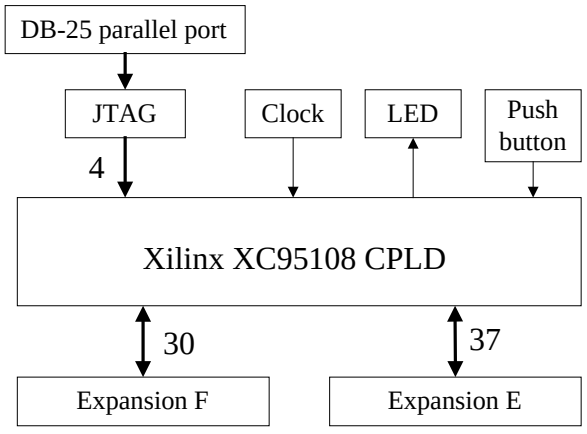
XC95108 CPLD

The block diagram of the DXC95 board shows all connections between the CPLD and the devices on

the board. All CPLD pin connections are shown in the table.

The CPLD device can be configured using the Xilinx JTAG tools and a parallel cable connecting the DXC95 board and the host computer.

For further information on the XC95108 CPLD, please see the Xilinx data sheets available at the Xilinx website (www.xilinx.com).



DXC95 CPLD circuit block diagram

Pin	Function	Pin	Function
1	LED1	43	E36
2	BTN1	44	E35
3	F29	45	E34
4	F28	46	E33
5	F27	47	E32
6	F26	48	E31
7	F25	49	**GND**
8	**GND**	50	E30
9	MCLK	51	E29
10	GCLK2	52	E28
11	F23	53	E27
12	GCK3	54	E26
13	F21	55	E25
14	F20	56	E24
15	F19	57	E23
16	**GND**	58	E22
17	F18	59	**TDO**
18	F17	60	**GND**
19	F16	61	E21
20	F15	62	E20
21	F14	63	E19
22	**VCCIO**	64	**VCCIO**
23	F13	65	E18
24	F12	66	E17
25	F11	67	E16
26	F10	68	E15
27	**GND**	69	E14
28	**TDI**	70	E13
29	**TMS**	71	E12
30	**TCK**	72	E11
31	F9	73	**VCCINT**
32	F8	74	GSR
33	F7	75	E10
34	F6	76	GTS1
35	F5	77	GTS2
36	F4	78	**VCCINT**
37	F40	79	E9
38	**VCCINT**	80	E8
39	F39	81	E7
40	F38	82	E6
41	F37	83	E5
42	**GND**	84	E4