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PRELIMINARY

Digilab XC95 Reference Manual

Revision: May 7, 2002

Overview

The Digilab XC95 (DXC95) development board featuring the Xilinx 95108 CPLD provides an inexpensive and expandable platform on which to design and implement basic digital circuits. The board can also be used to program other Digilent peripheral boards (such as the DIO2 board) that contain CPLD devices. DXC95 board features include:

- A Xilinx 95108 CPLD with 108 macrocells;
- An on-board 1.5A, 5VDC power regulator;
- A socketed 1.842MHz oscillator;
- A JTAG-based programming port using a standard parallel cable;
- A status LED and pushbutton for basic I/O;
- Two 100-mil spaced, right-angle DIP socket 40-pin expansion connectors.

The DXC95 board has been designed specifically to work with the Xilinx ISE CAD tools, including the free WebPack tools available from the Xilinx website. Like other in the Digilab family, the DXC95 board has been partitioned so that only the hardware required by a particular project need be purchased. Several peripheral boards that mate with the expansion connectors are available, such as the DIO1 board that provides several basic I/O devices (see www.digilentinc.com for more information). The low-cost, standard expansion connectors allow new peripheral boards, including wire-wrap or manually soldered boards, to be quickly designed and used. The DXC95 board ships with a power supply and programming cable, so designs can be implemented immediately without the need for any additional hardware.

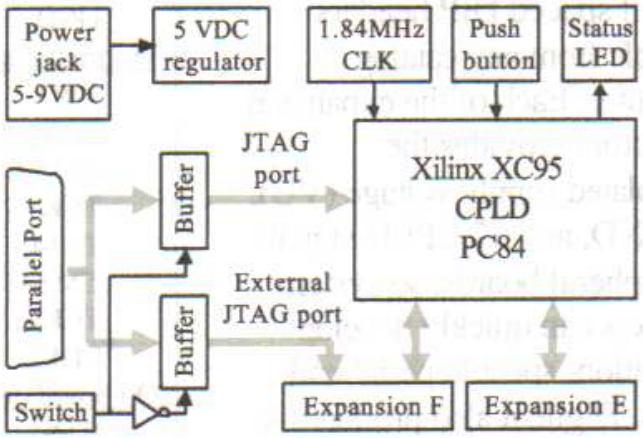
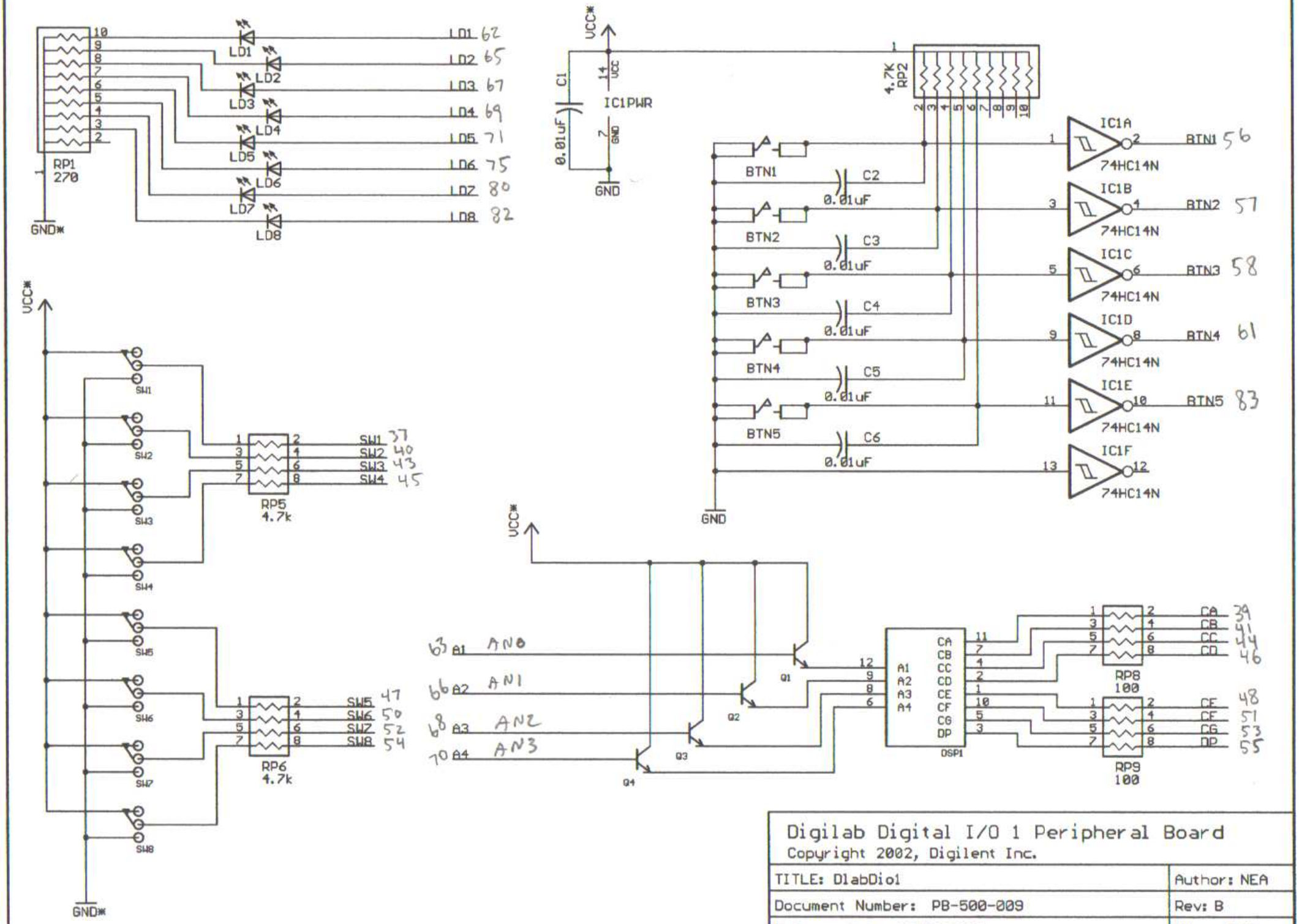


Figure 1. DXC95 board schematic



Digilab Digital I/O 1 Peripheral Board

TITLE: DlabDio1	Author: NEA
Document Number: PB-500-009	Rev: B
Release Date: 10/24/2002	Sheet: 2/2

Functional description

The Digilab DXC95 board has been designed to offer a low-cost and minimal system for designers who need a flexible platform to gain exposure to Xilinx CPLDs, or for those who need to prototype CPLD-based designs rapidly. The DXC95 board also has an external JTAG port – in a lower-cost configuration, the board can be used to program Digilab peripheral boards (such as the DIO2 or AIO1 boards). The DXC95 board provides only the essential supporting devices for the 95108 CPLD, and routes all available CPLD signals to standard expansion connectors. Included on the board are a 5VDC regulator, a JTAG configuration circuit that uses a standard parallel cable, a 1.8MHz oscillator, and a pushbutton and LED for rudimentary I/O.

The DXC95 board has been designed to serve as a host for various peripheral boards. The expansion connectors on the board mate with standard 40-pin, 100 mil spaced DIP headers available from any catalog distributor. Each of the expansion connectors provides the unregulated supply voltage (VU), 5V, GND, and 37 CPLD signals to peripheral boards, so system designers can quickly develop application- specific peripheral boards. Digilent also produces a collection of expansion boards with commonly used devices. See the Digilent website (www.digilentinc.com) for a listing of currently available boards.

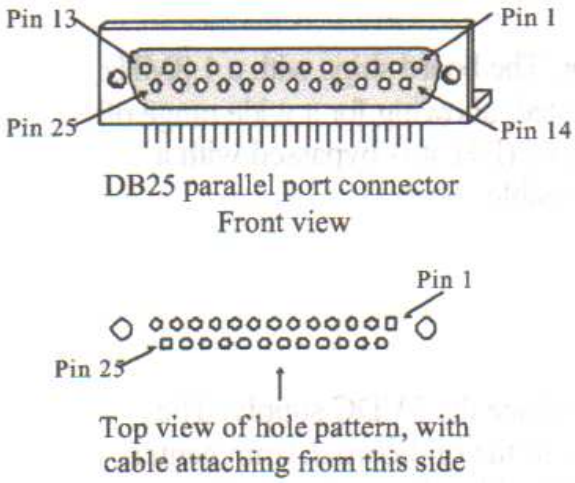
Power Supplies	
VU	Unregulated power supply voltage – depends on power supply used. Must be between 5VDC and 10VDC. Routed to regulators and expansion connectors only.
VCC	VCC for all devices, routed on inner PCB plane. 1.5A can be drawn with less than 20mV ripple (typical)
GND	System ground routed to all devices on PCB ground plane
Programming and parallel port	
PWT	Feedback of TDO signal
PPO	Cable detect signals used by Xilinx programmer
TMS-L	Local TMS signal (used for JTAG programming)
TCK-L	Local TCK signal (used for JTAG programming)
TDI-L	Local TDI signal (used for JTAG programming)
TMS-E	External TMS signal (used for JTAG programming)
TCK-E	External TCK signal (used for JTAG programming)
TDI-E	External TDI signal (used for JTAG programming)
On board devices	
BTN1	Pushbutton input
LED1	User-controllable status LED
MCLK	CMOS oscillator connected to global clock input
Expansion Connectors	
E4-E40	E bus signals connecting the E connector to the FPGA
F4-F40	F bus signals connecting the F connectors to the FPGA

Table 1. DXC95 board signal definitions

Table 1 shows all signals routed on the DXC95 board. These signals and their circuits are described in the following sections.

Parallel port and FPGA configuration circuit

The DXC95 board uses a DB-25 parallel port connector to route JTAG programming signals from a host computer to the CPLD and to the F expansion connector. Three-state buffers, controlled by an user-settable switch, determine whether the JTAG port is mapped to the on-board device or to the expansion connector. With this circuit, the on-board CPLD or a peripheral board CPLD can be configured using the JTAG protocol over the parallel cable. The JTAG programming circuit follows the schematic available from Xilinx, so the DXC95 board is fully compatible with all Xilinx programming tools. The JTAG circuit is shown in the diagram below.



Pin	EPP signal	EPP Function
1	Write Enable (O)	Low for read, High for write
2-9	Data bus (B)	Bidirectional data lines
10	Interrupt (I)	Interrupt/acknowledge input
11	Wait (I)	Bus handshake; low to ack
12	Spare	NOT CONNECTED
13	Spare	NOT CONNECTED
14	Data Strobe (O)	Low when data valid
15	Spare	NOT CONNECTED
16	Reset (O)	Low to reset
17	Address strobe (O)	Low when address valid
18-25	GND	System ground

Figure 1. Parallel port connectors and signals

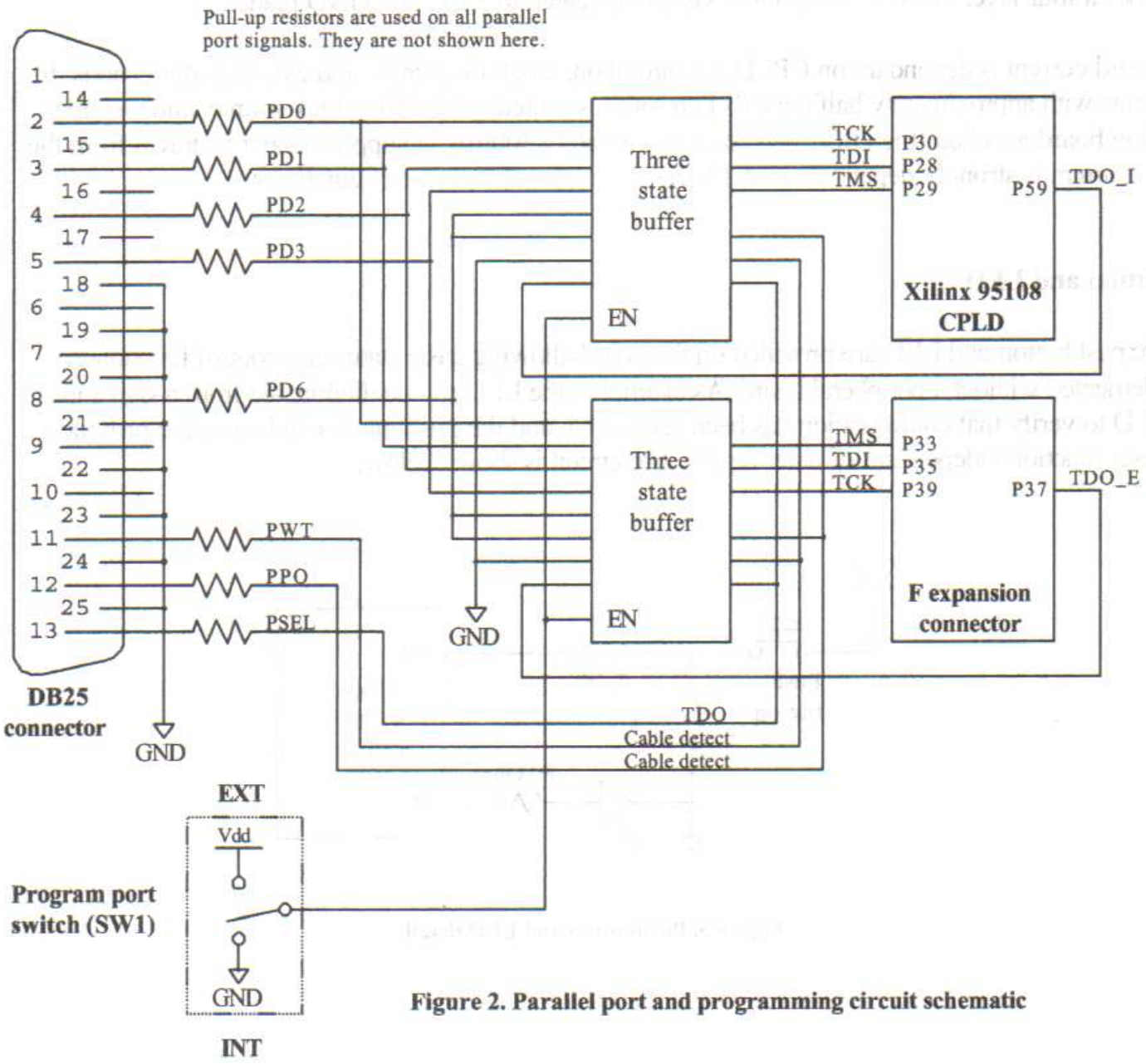


Figure 2. Parallel port and programming circuit schematic

Oscillator

The DXC95 board provides a socketed half-size 8-pin DIP oscillator. The board ships with a 1.8MHz oscillator, but oscillators from 32KHz to 50MHz can easily be substituted, allowing for a wide range of clock frequencies. The oscillator is connected to the CPLD GCK1 input (P9), it is bypassed with a 0.1uF capacitor, and it located as physically close to the CPLD as possible.

Power Supplies

The DCX95 board uses a 1.5A LM317 LDO voltage regulator to produce the 5VDC supply. The regulator input is driven from an external DC power supply connected to the on-board 2.1mm center-positive power jack. The regulator has 10uF of input capacitance, 20uF of local output capacitance, and 10uF of regulation bypass capacitance. The regulator produces a stable, low noise supply using inexpensive wall-wart power supplies, regardless of load (up to 1.5A). The regulator body is soldered to the board for improved thermal dissipation. DC supplies in the range of 5VDC to 10VDC may be used. Ample bypass capacitors are used around the board to decrease power supply noise. The DXC95 board uses a four layer PCB, with the inner layers dedicated to VCC and GND planes

Total board current is dependant on CPLD configuration, clock frequency, and external connections. In test circuits with approximately half the CPLD resources routed, a 1.8MHz clock source, and a single expansion board attached (the DIO1 board), approximately 300mA of supply current is drawn from the supply. Current is strongly dependent on CPLD and peripheral board configurations.

Pushbutton and LED

A single pushbutton and LED are provided on the board allowing basic status and control functions to be implemented without a peripheral board. As examples, the LED can be illuminated from a signal in the CPLD to verify that configuration has been successful, and the pushbutton can be used to provide a basic reset function independent of other inputs. The circuit is shown below.

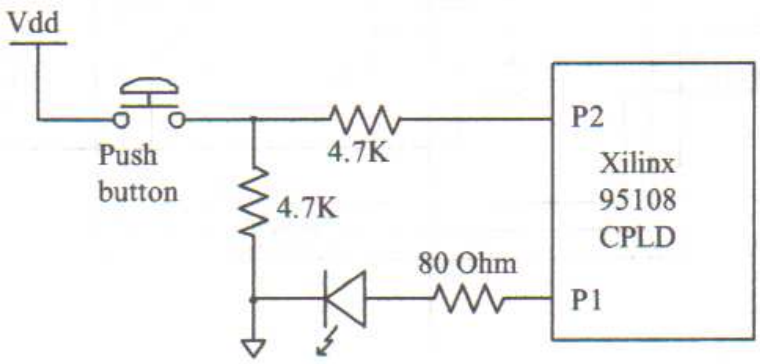
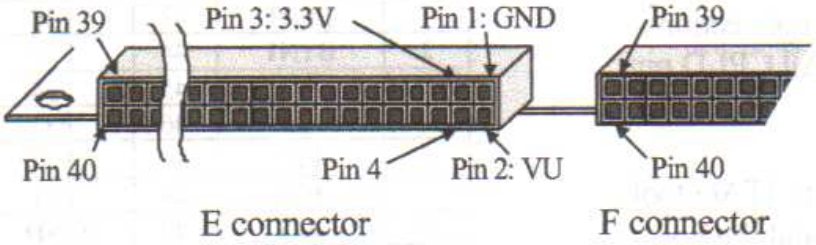


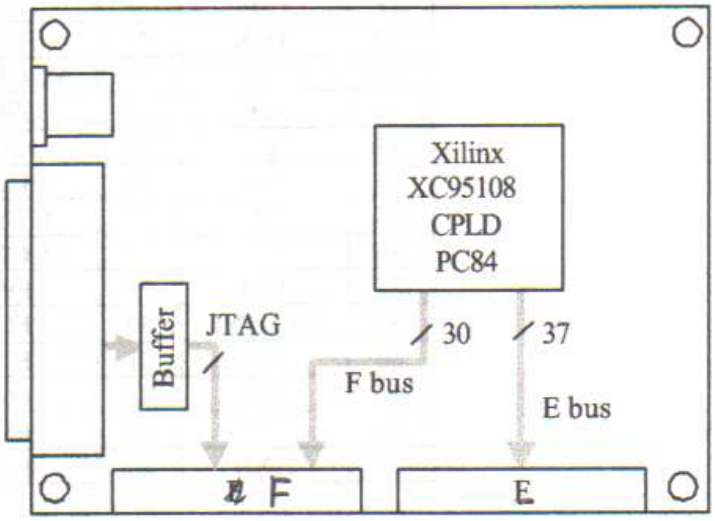
Figure 5. Pushbutton and LED detail

Expansion connectors



The two expansion connectors labeled E and F on the DXC95 board use 100 mil spaced DIP headers. Both connectors have GND routed to pin 1, VU routed to pin 2, and 5V routed to pin 3. Pins 4-40 for both connectors route directly to individual CPLD pins. The connectors are separated by 400 mils, so any Digilent peripheral board can be used with the DCX95 board.

The PC84 package used on the DXC95 board has 69 signal pins available to the user (the remaining pins are used for VCC, GND, and JTAG). Of these, 69, 3 are used for the button, led, and clock, and the rest are routed to the E and F peripheral connectors. Data rates of up to the full clock frequency are attainable across the E and F connectors.



DXC95 expansion connector signals

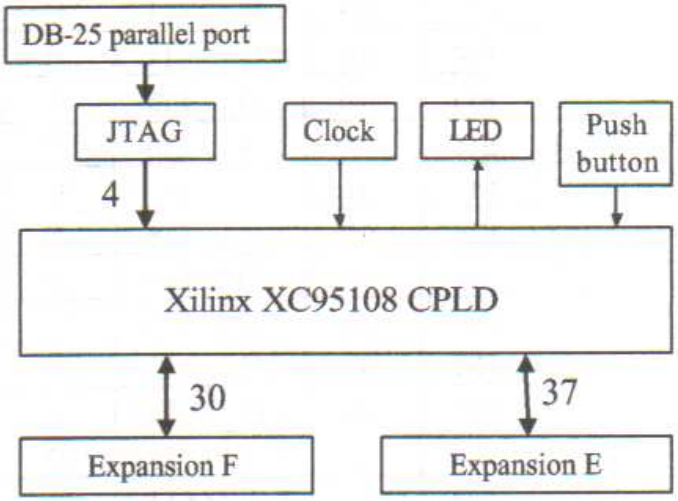
DXC95 Expansion Connector Pinouts					
E connector			F connector		
Pin	Signal	S-II pin	Pin	Signal	S-II pin
1	GND	-	1	GND	-
2	VU	-	2	VU	-
3	VDD33	-	3	VDD33	-
4	E4	122	4	F4	56
5	E5	121	5	F5	54
6	E6	120	6	F6	51
7	E7	118	7	F7	50
8	E8	117	8	F8	49
9	E9	115	9	F9	48
10	E10	114	10	F10	47
11	E11	113	11	F11	46
12	E12	112	12	F12	44
13	E13	103	13	F13	43
14	E14	102	14	F14	41
15	E15	100	15	F15	40
16	E16	99	16	F16	31
17	E17	96	17	F17	30
18	E18	95	18	F18	29
19	E19	94	19	F19	28
20	E20	93	20	F20	27
21	E21	87	21	F21	26
22	E22	86	22	GCLK3	23
23	E23	85	23	F23	22
24	E24	84	24	GCLK2	21
25	E25	83	25	F25	20
26	E26	80	26	F26	19
27	E27	79	27	F27	13
28	E28	78	28	F28	12
29	E29	77	29	F29	11
30	E30	75	30	BTN1	10
31	E31	74	31	MCLK	7
32	E32	67	32	LED1	6
33	E33	66	33	TMS_E	5
34	E34	65	34	GTS1	4
35	E35	63	35	TDI_E	3
36	E36	62	36	GSR	76
37	E37	60	37	TDO_E	64
38	E38	59	38	GTS2	42
39	E39	58	39	TCK_E	88
40	E40	57	40	F40	18

XC95108 CPLD

The block diagram of the DXC95 board shows all connections between the CPLD and the devices on the board. All CPLD pin connections are shown in the table.

The CPLD device can be configured using the Xilinx JTAG tools and a parallel cable connecting the DXC95 board and the host computer.

For further information on the XC95108 CPLD, please see the Xilinx data sheets available at the Xilinx website (www.xilinx.com).



DXC95 CPLD circuit block diagram

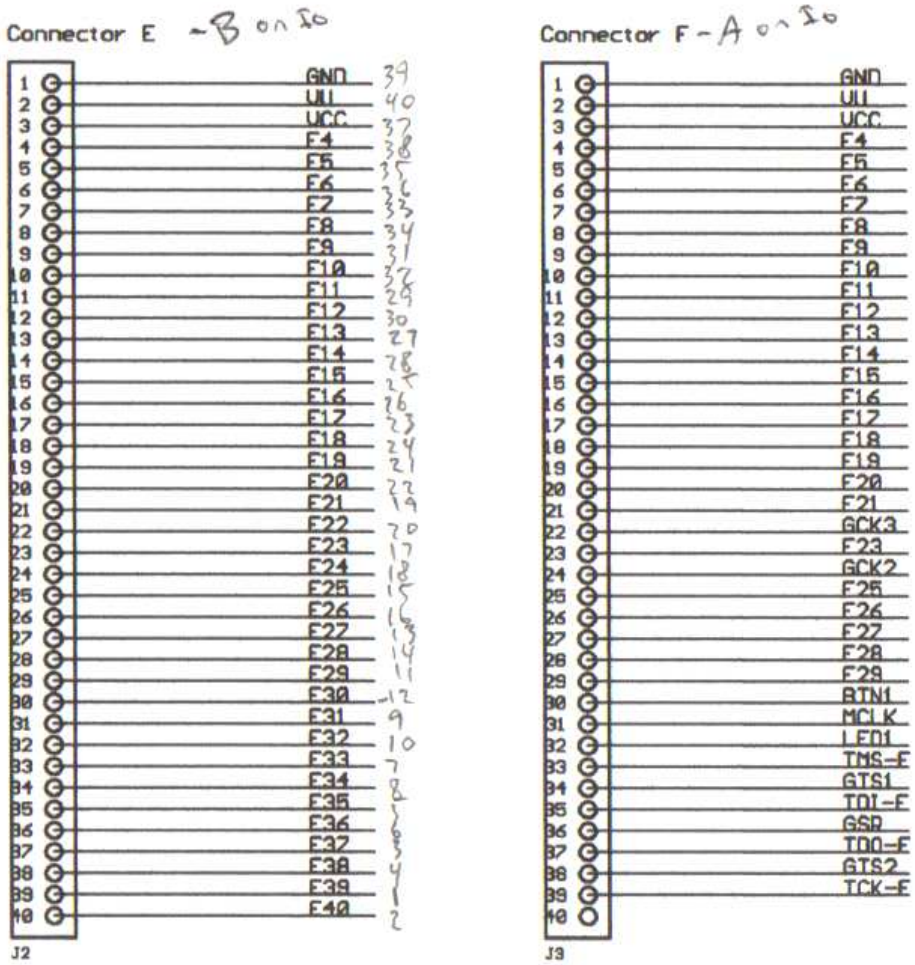
CPLD CPLD

Pin	Function	Pin	Function
1	LED1	43	F36
2	BTN1	44	F35
3	E29	45	F34
4	E28	46	F33
5	E27	47	F32
6	E26	48	F31
7	E25	49	**GND**
8	**GND**	50	F30
9	MCLK	51	F29
10	GCLK2	52	F28
11	E23	53	F27
12	GCK3	54	F26
13	E21	55	F25
14	E20	56	F24
15	E19	57	F23
16	**GND**	58	F22
17	E18	59	**TDO**
18	E17	60	**GND**
19	E16	61	F21
20	E15	62	F20
21	E14	63	F19
22	**VCCIO**	64	**VCCIO**
23	E13	65	F18
24	E12	66	F17
25	E11	67	F16
26	E10	68	F15
27	**GND**	69	F14
28	**TDI**	70	F13
29	**TMS**	71	F12
30	**TCK**	72	F11
31	E9	73	**VCCINT**
32	E8	74	GSR
33	E7	75	F10
34	E6	76	GTS1
35	E5	77	GTS2
36	E4	78	**VCCINT**
37	F40	79	F9
38	**VCCINT**	80	F8
39	F39	81	F7
40	F38	82	F6
41	F37	83	F5
42	**GND**	84	F4

Digilab Digital I/O 1, Rev B to Digilab XC95

DIO1B Pin	Signal	XC95 Pin	Signal	CPLD Pin
A1		F39	TCK	
A2		F40		
A3		F37	TDO	
A4		F38	GTS2	77
A5		F35	TDI	
A6		F36	GSR	74
A7		F33	TMS	
A8		F34	GTS1	76
A9		F31	MCLK	9
A10		F32	LED1	1
A11		F29	F29	3
A12		F30	BTN1	2
A13		F27	F27	5
A14		F28	F28	4
A15		F25	F25	7
A16		F26	F26	6
A17		F23	F23	11
A18		F24	GCK2	10
A19		F21	F21	13
A20		F22	GCK3	12
A21		F19	F19	15
A22		F20	F20	14
A23		F17	F17	18
A24		F18	F18	17
A25		F15	F15	20
A26		F16	F16	19
A27		F13	F13	23
A28		F14	F14	21
A29		F11	F11	25
A30		F12	F12	24
A31	BLU	F9	F9	31
A32	PS2D	F10	F10	26
A33	GRN	F7	F7	33
A34	PS2C	F8	F8	32
A35	RED	F5	F5	35
A36	HS	F6	F6	34
A37	VCC	F3	VCC	
A38	VS	F4	F4	36
A39	GND	F1	GND	
A40	VU	F2	VU	

DIO1B Pin	Signal	XC95 Pin	Signal	CPLD Pin
B1	CA	E39	E39	39
B2	SW1	E40	E40	37
B3	CB	E37	E37	41
B4	SW2	E38	E38	40
B5	CC	E35	E35	44
B6	SW3	E36	E36	43
B7	CD	E33	E33	46
B8	SW4	E34	E34	45
B9	CE	E31	E31	48
B10	SW5	E32	E32	47
B11	CF	E29	E29	51
B12	SW6	E30	E30	50
B13	CG	E27	E27	53
B14	SW7	E28	E28	52
B15	DP	E25	E25	55
B16	SW8	E26	E26	54
B17	BTN2	E23	E23	57
B18	BTN1	E24	E24	56
B19	BTN4	E21	E21	61
B20	BTN3	E22	E22	58
B21	A1	E19	E19	63
B22	LD1	E20	E20	62
B23	A2	E17	E17	66
B24	LD2	E18	E18	65
B25	A3	E15	E15	68
B26	LD3	E16	E16	67
B27	A4	E13	E13	70
B28	LD4	E14	E14	69
B29		E11	E11	72
B30	LD5	E12	E12	71
B31		E9	E9	79
B32	LD6	E10	E10	75
B33		E7	E7	81
B34	LD7	E8	E8	80
B35	BTN5	E5	E5	83
B36	LD8	E6	E6	82
B37	VCC	E3	VCC	
B38	LDG	E4	E4	84
B39	GND	E1	GND	
B40	VU	E2	VU	



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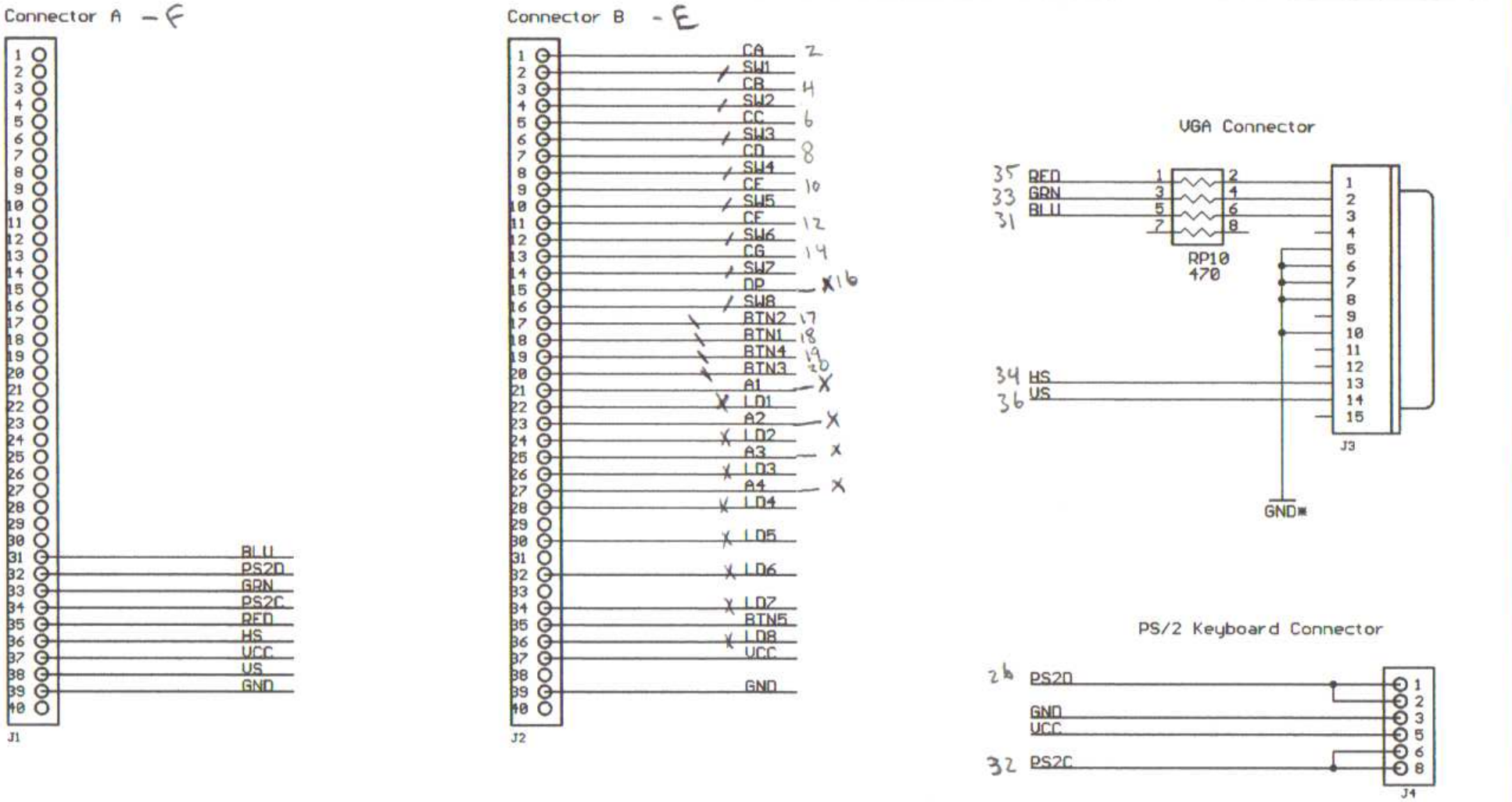
Digilab Digital I/O 1, Rev B to Digilab XC95

DIO1B Pin	Signal	XC95 Pin	Signal	CPLD Pin
A1		F39	TCK	
A2		F40		
A3		F37	TDO	
A4		F38	GTS2	77
A5		F35	TDI	
A6		F36	GSR	74
A7		F33	TMS	
A8		F34	GTS1	76
A9		F31	MCLK	9
A10		F32	LED1	1
A11		F29	F29	3
A12		F30	BTN1	2
A13		F27	F27	5
A14		F28	F28	4
A15		F25	F25	7
A16		F26	F26	6
A17		F23	F23	11
A18		F24	GCK2	10
A19		F21	F21	13
A20		F22	GCK3	12
A21		F19	F19	15
A22		F20	F20	14
A23		F17	F17	18
A24		F18	F18	17
A25		F15	F15	20
A26		F16	F16	19
A27		F13	F13	23
A28		F14	F14	21
A29		F11	F11	25
A30		F12	F12	24
A31	BLU	F9	F9	31
A32	PS2D	F10	F10	26
A33	GRN	F7	F7	33
A34	PS2C	F8	F8	32
A35	RED	F5	F5	35
A36	HS	F6	F6	34
A37	VCC	F3	VCC	
A38	VS	F4	F4	36
A39	GND	F1	GND	
A40	VU	F2	VU	

DIO1B Pin	Signal	XC95 Pin	Signal	CPLD Pin
B1	CA	E39	E39	39
B2	SW1	E40	E40	37
B3	CB	E37	E37	41
B4	SW2	E38	E38	40
B5	CC	E35	E35	44
B6	SW3	E36	E36	43
B7	CD	E33	E33	46
B8	SW4	E34	E34	45
B9	CE	E31	E31	48
B10	SW5	E32	E32	47
B11	CF	E29	E29	51
B12	SW6	E30	E30	50
B13	CG	E27	E27	53
B14	SW7	E28	E28	52
B15	DP	E25	E25	55
B16	SW8	E26	E26	54
B17	BTN2	E23	E23	57
B18	BTN1	E24	E24	56
B19	BTN4	E21	E21	61
B20	BTN3	E22	E22	58
B21	A1	E19	E19	63
B22	LD1	E20	E20	62
B23	A2	E17	E17	66
B24	LD2	E18	E18	65
B25	A3	E15	E15	68
B26	LD3	E16	E16	67
B27	A4	E13	E13	70
B28	LD4	E14	E14	69
B29		E11	E11	72
B30	LD5	E12	E12	71
B31		E9	E9	79
B32	LD6	E10	E10	75
B33		E7	E7	81
B34	LD7	E8	E8	80
B35	BTN5	E5	E5	83
B36	LD8	E6	E6	82
B37	VCC	E3	VCC	
B38	LDG	E4	E4	84
B39	GND	E1	GND	
B40	VU	E2	VU	



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TITLE: DlabDio1	Author: NEA
Document Number: PB-500-009	Rev: B
Release Date: 10/24/2002	Sheet:1/2